PRELIMINARY

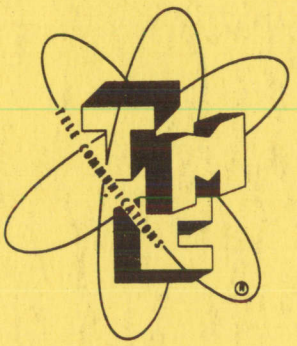
TECHNICAL MANUAL

EXCITER EQUIPMENT

MODEL AX-239

FOR

SIDEBAND TRANSMITTERS



THE TECHNICAL MATERIEL CORP.

Mamaroneck, N. Y. Ottawa, Ontario

- NOTICE -

The 1 megacycle standard in this equipment requires a minimum continuous operational period of 48 hours to fully establish and maintain its rated stability. At the end of this period the stability will be 1 part in 10^8 per day under normal fixed station operating conditions.

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SIDEBAND TRANSMITTERS

THE TECHNICAL MATERIEL CORPORATION

MAMARONECK, NEW YORK OTTAWA, CANADA

December 1, 1960

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PART I

GENERAL DESCRIPTION OF EXCITER

I-1-1 Introduction

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PART II

SIDEBAND GENERATOR MODEL SBG-1

SECTION I

GENERAL DESCRIPTION

II - 1-1. Introduction

II - 1-2. Functional Description of SBG-1 Units.

II - 1-1-3. Reference Data.

SECTION II

INSTALLATION

II- 2-1. General

a. As shown in table 1-(), the AX-239 is shipped in () wooden cases. On arrival, uncrate each and carefully inspect for damage. If any damage is found, notify the carrier or supply department immediately. Inspect all packing material for parts shipped as loose items.

b. The contents of the () cases are packaged according to military specifications. The units are wrapped to avoid being scratched, placed in cartons, cushioned against shock, and wrapped and sealed with waterproof material within which the units are kept dry with a desiccant.

C. Figure II - 2-1 shows wiring details for the interconnection of the AX-239 rack-mounted units.

II - 2-2. Production Line Checkout.

Before any AX-239 is shipped, it has been assembled on the test floor and thoroughly checked against the manufacturer's test specifications. This procedure eliminates assembly line errors and guarantees that an AX-239 shall fully satisfy all design requirements. After this thorough checkout, the AX-239 is disassembled and packed for customer use. The packaging operations, in turn, is such as to minimize troubles that may develop in transit.

II - 2-3. Location of AX-239

Ordinarily, the AX-239 is an auxiliary frame chassis to the GPT-10K and GPT-40K transmitters. Locations of the AX-239, therefore, is governed by associated transmitter equipment. The installation details of the transmitter equipment, therefore, govern those of the AX-239. Installation details of the transmitter equipment are given in pertinent technical manuals on the transmitters.

II - 2-4. Assembly of AX-239.

After the AX-239 is unpacked and located as discussed in paragraphs 2-1, 2-2, and 2-3 above, the modular units are inserted in the exciter frame and 115/230 volt 50/60 cycle power is connected to the AX-239 as indicated in figure II - 2-1. However, before turning power on the AX-239, continuity checks should be made between terminals in line with information on figure II - 2-1. Inspection should be made for loose/broken connections.

II - 2-5. Installation Checkout.

To come later.

SECTION III

OPERATOR's SECTION

To come later.

SECTION IV

PRINCIPLES OF OPERATION

4-1 General.

As explained in Section I, the modular-type construction of the Sideband Generator Model SBG-1 makes it convenient to describe the principles on a building block basis. However, to facilitate understanding, some general remarks are pertinent.

a. Automatic Phase Control System.

As shown in following figure II - 4-1, the system contains as oscillator with a nominal frequency equal to the desired output frequency; some form of reactance modulator or other means of voltage control of the oscillator frequency; a phase detector which compares the outputs of the oscillator and the reference source; and a low-pass filter which filters the output voltage of the phase detector before it is applied to the reactance modulator

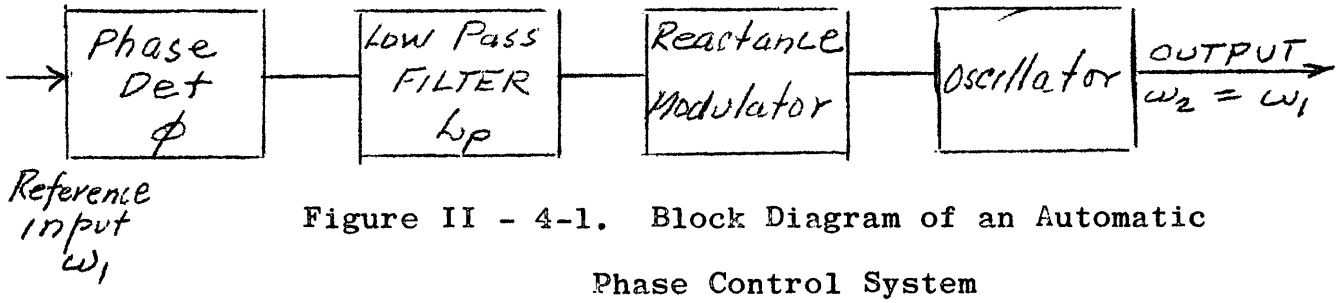
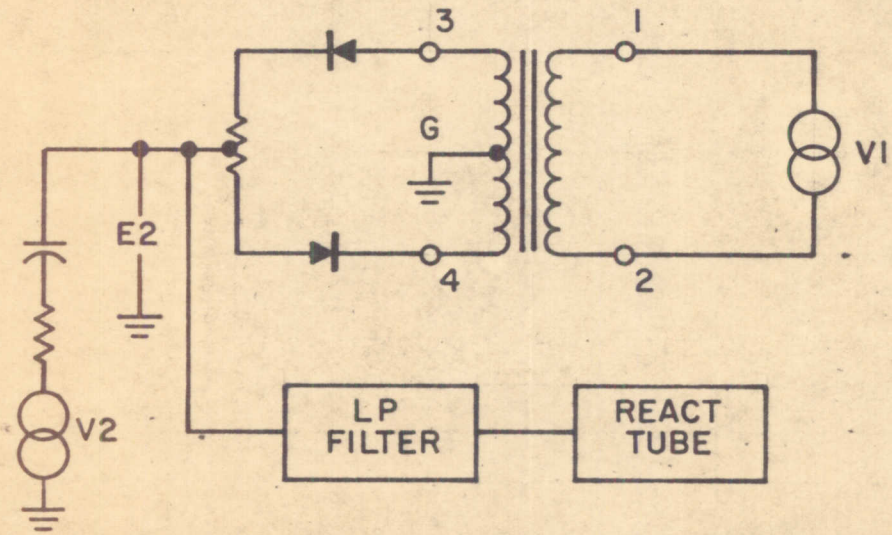


Figure II - 4-1. Block Diagram of an Automatic Phase Control System

The operation of the system can be understood quallititively by assuming that the oscillator frequency is equal to that of the reference. The phase-detector output is then a DC voltage dependent on the phase difference between the output signals of the oscillator and the reference. This foltage is applied through the low-pass filter to the

reactance modulator and thereby governs the oscillator frequency. If the oscillator frequency tends to change this attempted change is first felt as a phase-difference change in the phase detector. This produces a change in phase-detector output voltage which acts to hold the oscillator frequency constant. As the oscillator drifts, its output phase, relative to that of the reference, will drift byt its average frequency will remain fixed. The system operates exactly like a positional servomechanism wherein, for constant input position, the output position is exactly equal to the input, with zero steady state error.

b. Phase Detector Circuit. As shown in following figure II-4-3, voltage V1 produces voltage E1 across the potenticmeterR. When terminal 3 is positive relative to terminal 4, the diodes conduct and present a relatively low impedance; when terminal 3 is negative relative to terminal 4, the diodes are non-donducting and present a very high impedance.



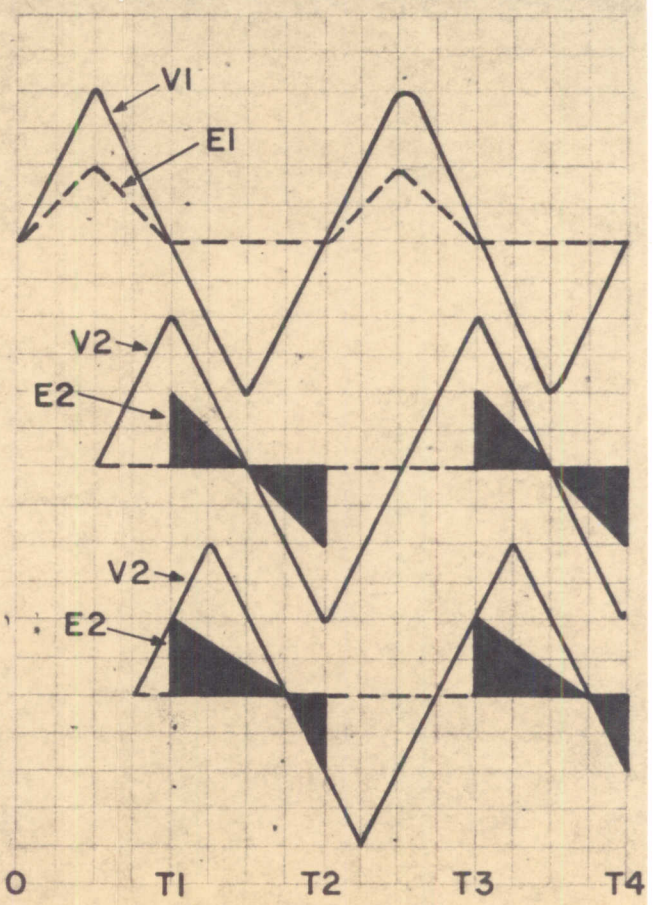


FIGURE II-4-2

SIMPLIFIED SCHEMATIC DIAGRAM ILLUSTRATING OPERATION OF PHASE DETECTOR CIRCUIT USED IN CONTROLLED PRECISION OSCILLATOR.

Now, let V2's frequency be the same as V1's frequency but V2's phase be 90 degrees behind V1's phase. For clarity, V2's zero axis (Figure II - 4-2) is displaced below V1's zero axis. During the first and third half cycles of V1, V2 "Sees" G through the relatively low impedance of the diodes. During the second and fourth half cycles of V1, V2 "Sees" G through the very high impedance of the diodes. The wave shape of E2 is as shown with equal positive and negative areas of voltage at the LP filter's input.

Now, let V2's frequency be the same as V1's frequency but V2's phase be 135 degrees behind V1's phase. For clarity, V2's zero axis is displaced below V1's zero axis. Again, during times 0 T_1 and T_2T_3, when the diodes are conducting, the value of E2 is substantially zero. During times T_1T_2 and T_3T_4, when the diodes are non-conducting, the value of E2 is positive or negative depending upon phase. The wave shape of E2 is as shown with unequal positive and negative areas of voltage at the LP filter's input.

a. Frequency Translations in High Frequency and Low Frequency Loops.

Figure II-4-3 is a block diagram illustrating a particular procedure of frequency translations in high frequency and low frequency loops. The procedure used in the SBG-1 differs in its details from that shown on figure II-4-3; however, this is of small importance in the general understanding of the SBG-1, as will be seen from the discussions presented in later paragraphs.

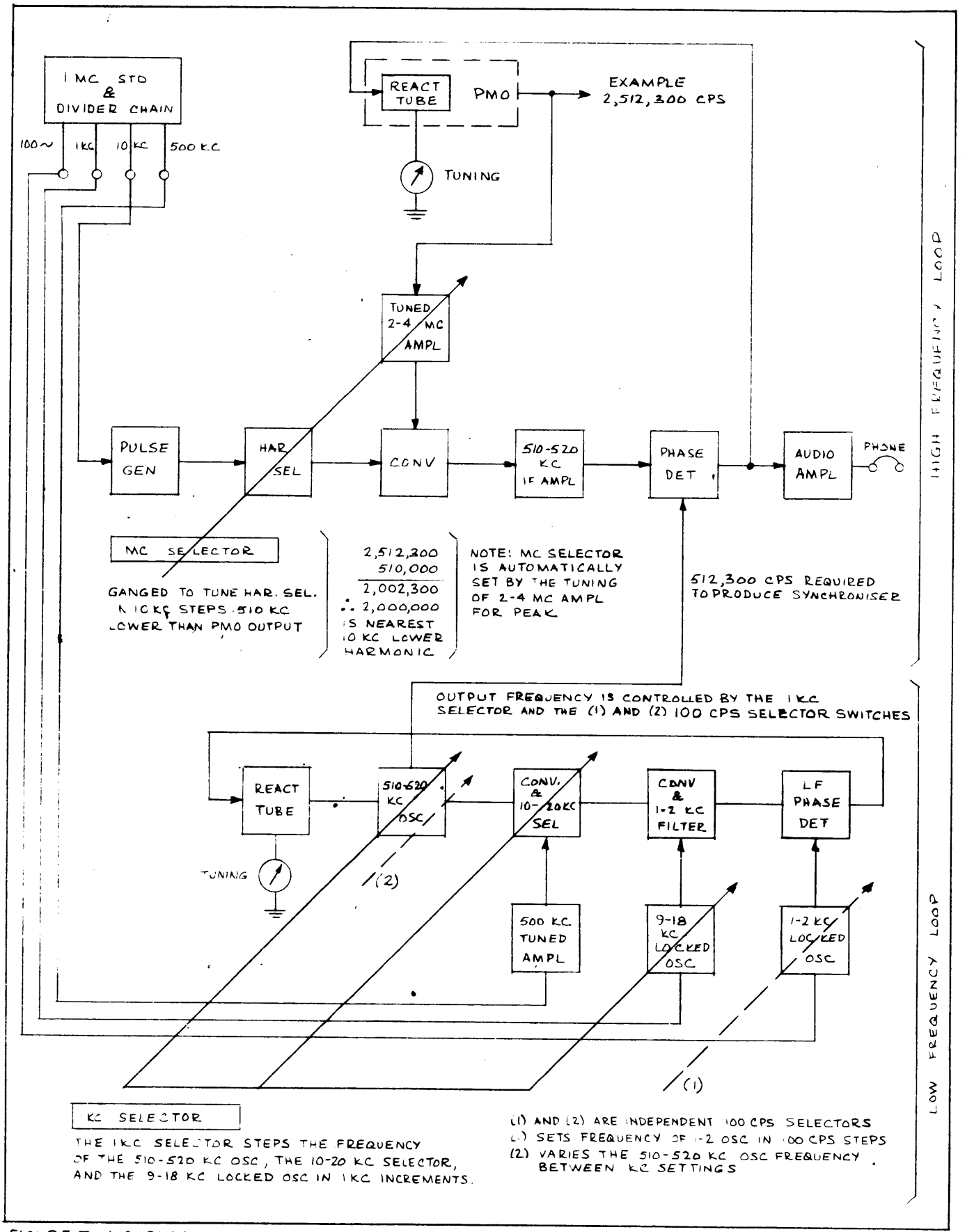


FIGURE II-4-3 BLOCK DIAGRAM ILLUSTRATING FREQUENCY TRANSLATION IN HIGH FREQUENCY AND LOW FREQUENCY LOOPS

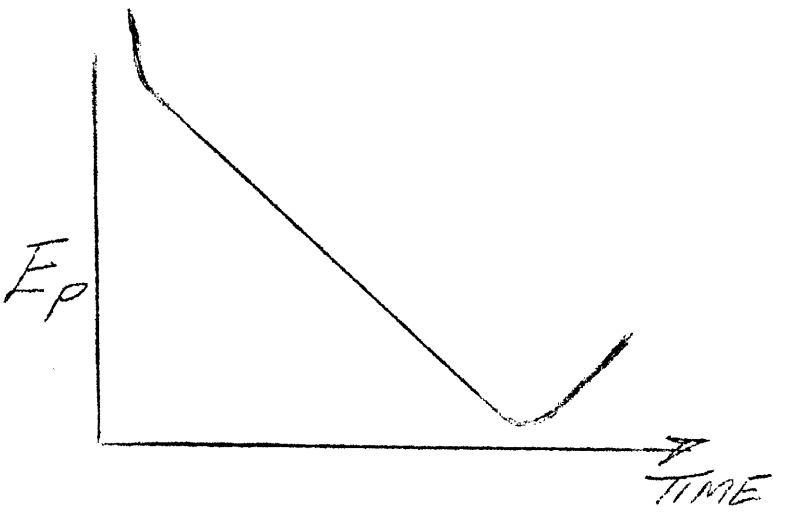
To simplify the analysis, assume PMO's output is to be exactly 2, 512, 300 cps. The output of the PMO is fed to a converter via a tuned 2-4 megacycle amplifier. The output of the converter is fed to a 510-520 Kc IF amplifier. If the output of the harmonic selector (10 Kc steps) is 2,000,000 cps and that of the PMO is approximately 2,512,300 cps, the output of the converter is in the range of the 510-520 Kc IF amplifier. This result is obtained by tuning the TUNED 2-4 Mc AMPL for peak reading by the MC SELECTOR knob, which simultaneously peaks the amplifier's output and selects the PULSE GEN'S 10 Kc harmonic 510-520 Kc below the PMO's frequency; in the case at hand, 2000 Kc. Thus one terminal of the PHASE DET receives an approximate 512,300 cps. To adjust the PMO's frequency to exactly 2,512,200 cps, the low frequency loop provides the PHASE DET with a voltage of exactly 512,300 cps. The PHASE DET DC output thereby adjust the PMO's frequency to exactly 2,512,300 cps via its REACT TUBE.

It now remains to be seen how the low frequency loop provides the high frequency loop's PHASE DET with a voltage of exactly 512,200 cps. The low frequency loop's CONV and 10-20 Kc SEL heterodynes two incoming voltages, one from the phase-locked 510-520 Kc OSC and the other from a precision 500 Kc standard via the 500 KC TUNED AMPL. If the 1 Kc SELECTOR is set for 2 Kc and the 100 cps SELECTOR is set for 1300 cps, the system is stabilized only when both inputs to the LF PHASE DET have frequencies of 1300 cps. With a 25 Kc setting of the 1 Kc SELECTOR, the 9-18 Kc LOCKED OSC has an output frequency of 11 Kc. Therefore the output frequency of the CONV & 10 SEL must be 12,300 cps and the output frequency of the phase locked 510-520 Kc OSC must be 512,300 cps.

D. Frequency Division by Phantastrons.

Frequency division is sometimes obtained by driving a multivibrator with a synchronizing voltage well beyond the multivibrator's natural frequency. As an attempt is made to pull the multivibrator to higher and higher frequencies, a limit is reached beyond which the multivibrator synchronizes to one half of the driving frequency. Similarly, the multivibrator may synchronize to one-third or even a smaller fraction of the driving frequency. The advantage of th phantastron delay multivibrator over the usual types of delay circuits or multivibrators is the direct relationship between the controlling voltage and the delay time as compared to an exponential relationship in the usual circuits.

A phantastron circuit composed of a single multigrid tube may be considered the equivalent of two-tube circuit wherein one tube consists of the cathode, control grid A, and shield grid(acting as plate) and the other tube consists of the cathode, control grid B,(phantom) control grid A, and plate. As the cathode is common to both tubes, the electrons going to the plate are controlled by both grid B and phantom control grid A. The cumulative effect causes the plate voltage to decrease at a relatively slow and linear rate as shown in the following wave shape diagram.



4-2. Sideband Exciter, Model CBE-1 (Part of SBG-1) Figure II - 4-4.

The CBE-1 accepts two channels of intelligence (each having a bandwidth of 7.5 Kc) and processes them for sideband transmission in the frequency range 1.75 - 33.75 Megacycles.

Black diagram, figure II - 4-4, shows how the result is accomplished. Schematic figure II - 7-1, elaborates on the technical details The final technical manual will present stage-by-stage descriptions based on simplified schematic diagrams; this preliminary technical manual is limited to block diagram descriptions.

Audio-frequency amplifiers V203 and V207 receive intelligence in channels 1 and/or 2. This intelligence is frequency translated into sideband around 250 Kc carrier by a 250 Kc carrier input supply and sideband modulators, amplifiers, and filters. The output of the carrier rejection network Z202 contains the two 7.5 Kc bandwidths of intelligence with the 250 Kc carrier rejected, unless re-inserted by CARRIER REINSERT resistor R236. POwer amplifier PA 206 raises the power output to watts (PEP).

M201 and M202 monitor levels to guard against distortion. The exciter has self contained power supplies.

4-3 Power Supply, Model CPP-1 (Part of SBG-1), Figure II - 4-5.

The power supply for component Model CHG of SBG-1 requires 200-volt unregulated and 150-volt regulated outputs. Block diagram, figure II 4-5, shows how the result is accomplished. Schematic, Figure II - 7-2 elaborates on the technical details.

4-4 High Frequency Loop, Model CHG-1 (Part of SBG-1), Figure II-4-5.

Refer to paragraph 4-1.C in this part of the manual for the role played by SBG-1's high frequency loop model CHG. Block diagrams, figure II - 4-6 and II - 4-7, will show the techniques used in SBG-1 and schematic diagram, figure II - 7-3, will show the details.

Refer to figure II - 4-6. The output of the high frequency loop on band 1, is 1.75 to 3.75 mc; on band 2, 3-75 to 5.75 mc; and finally on band 16, 31.75 to 33.75 mc.

Inside the finely-engineered double oven are crystals and capacitors which are closely associated with an external high-frequency oscillator (HFO) V1303/V1304 and vari-capacitor C1319. The megacycle output (Amc) of V1303/V1304 ranges from 9 and 16 in precise megacycles frequencies (see note 1 of figure II - 4-6), under control of a synthesized feedback loop and vari-capacitor C1319, a solid-state device, whose capacitance varies with d-c input. The oven and oscillator chassis also contains 1 mc components comprising a spare "internal" 1 mc oscillator (V1302A), a 1 mc amplifier (V1302B) for J1303 and J1304; and a second 1 mc amplifier (V1303) for J1302. A more detailed block diagram for the CHG than figure II - 4-6 is given on figure II - 4-7. Details are given on schematic diagram figure II - 7-3.

The synthesizer chassis comprises incoming 1 mc and A mc input circuits, a 2 mc output circuit and a phase-detected d-c feedback circuit that controls the impedance of vari-capacitor C1319 mentioned in the preceding paragrph. Again, figure II - 4-7 elaborates on figure II - 4-6. The function of the synthesizer is to stabilize two CHG's outputs namely 2 mc and A mc, based on CHG's 1 mc standard input. The

components of the synthesizer compriseiisolation amplifier (V1501), harmonic generator (V1502), mixer (V1508), synchronizing indicator (V1504), doubler (V1505), and phase detector (T1501). These components are conventional and require no explanation other than, perhaps, phase detector circuit T1501 which is covered in preceding paragraph 4-1.b.

The IF chassis consists of incoming 2 mc and 1.75 - 3.75 mc circuits and an outgoing 14.25 - 16.25 mc circuit. The IF chassis contains an 18 mc generator V1201, an 18-mc amplifier V1202, a balanced modulator (CR1201, 1202), and 14.25 - 16.25 amplifiers V1204, V1205, and V1206. The arrangement is shown on figure II - 4-7; methods of operation are conventional.

The mid-frequency and HF deck chassis has four inputs and two outputs as follows:

a. 2-4 mc master oscillator CMO-1, described in paragraph 4-5 below.

b. Audio Sideband intelligence via CBE-1, described in paragraph 4-2 above.

c. Outgoing 1.75-3.75 mc sideband intelligence for frequency translation in the 14.25-16.25 mc frequency range.

d. Incoming 14.25 - 16.25 mc sideband intelligence per preceding item C.

e. Incoming a mc from the high frequency loop CHG in accordanne with preceidng paragraphs.

f. 1.75 - 33.75 mc outgong sideband intelligence to associated siddband transmitter.

Block diagrams, figure II - 4-6 and II - 4-7 show the circuit arrangements which are conventional, and figure II - 7-3 shows circuit details.

4-5 Master Oscillator, Model CMO-1 (Part of SBG-1) Figure II - 4-8.

As shown by figure II - 4-6, master oscillator CMO, when frequency stabilized, together with sideband exciter CBE, furnish the basic voltages for the associated sideband transmitter. Since CMO's frequency range is 2-4 mc, frequency translations, by additional precise heterodyning voltages, are needed. These are furnished by the MID-FREQUENCY & DECK assembly of the high frequency loop model CHG, as explained in preceding paragraph 4-4.

Figure II -4-8 shows the method by which master oscillator CMO is frequency stabilized. The frequency - stabilized feedback loop begins at V301, ½V302, goes to V304, and the MIXER V309. In the mixer the master oscillator's frequency is heterodyned by a harmonic derived from divider chain CHL's 10 Kc precision output. The heterodyned frequency is matched by low frequency loop CLL's 510-519.9 precision output, in phase detector V310. Phase detector V310's d-c output stabilized the ma ter oscillator's frequency by the means just indicated. Master Oscillator's RF output reaches J305, J306 via RF AMPL V304 and PA V305.

Mixer V312 provides a means of checking the master oscillator's frequency by comparison against a harmonic of a 100 Kc crystal oscillator.

4-6 Low Frequency Loop, Model CLL-1 (Part of SBG-1), Figure II - 4-9.

Refer to paragraph 4-1.c in this part of the manual for the role played by SBG-1's low frequency loop, model CLL-1. Block diagram, figure II - 4-9, will show the techniques used in SBG-1 and schematic diagram, Figure II - 7-5, will show the details.

The CLL-1 consists of three loops L1 (1000-1900 cps in 100 cps steps), L2 (9-18 Kc in 1 Kc steps), and L3 (510-519.9 Kc in 100 cps steps), in addition to a monitoring oscilloscope circuit. The end product of the CLL-1 are voltages in 100 cps steps in the range 510-519.9 Kc. These voltages are fed to the high frequency loop (CHG-1), where they are used, along with CMO and CBE voltages, to produce precise exciter voltages (intelligence) for an associated radio sideband transmitter operating in the 2-32 mc range.

In the L1 loop, two frequency-precise incoming voltages of 100 cps and 10 Kc from the divider chain (CHL-1) are used to provide L3 loop with precise 1 - 1.9 Kc voltages. Converter V707 is fed by a 10 Kc-precise voltage as well as a reactance - tube - controlled 11-11.9 oscillator output voltage. A phase detector assembly compares the converter's 1-1.9 Kc product withthe proper 100 cps harmonic (100 cps input and harmonic selector V705). The 11 -11.9 oscillator's frequency feedback circuit , comprising the above - referenced precise 100 cps harmonic, phase detector, and reactance tube V706A, enables V706 B to supply converter V707 with precision voltages as desired in the 11-11.9 Kc range in 100 cps steps. Selector switch S702 is the operators means employed to obtain this end result.

In the L2 loop, precise 9-18 Kc frequencies are produced by oscillator V702B/amplifier V703A by means of a frequency-controlled feedback circuit referenced by divider chain C11's 1 Kc standard. Refer to paragraph 4-1.a for technical explanation. Selector switch S701 is the operator's means employed to select the precise 1 Kc voltage wanted by the L3 loop, in the 9-18 Kc frequency range.

In the L3 loop, the products of the L1 and L2 loops are utilized to obtain precision voltages as desired in the 510-519.9 Kc range in 100 cps steps. As shown in figure II - 4-8, this range of precision voltages are supplied to the Master Oscillator CMO-1. Thus the low frequency loop CLL-1 controls CMO-s output, frequency-precise, in the 2-4 mc range in 100 cps steps, while the high frequency loop CHG-1 (figure II - 4-6) frequency-translates the 2-4 mc voltages to 1.75 - 33.75mc voltages. These are adequate to excite an associated transmitter operating in the 2 - 32 mc range.

The 510 - 520 Kc oscillator is under frequency control of reactance tube V708A and selector switches S701, S702. Its output feeds converter V709 which also receives a 500 Kc frequency-precise voltage from divider chain CLL. The converter's output, therefore, is a voltage from divider chain CLL. The converter's output, therefore, is a voltage in the 10-20 Kc range which is fed to a second converter V704 that also receives a 9-18 Kc frequency-precise voltage from loop 2 of CLL-1. V704's output, therefore , is a voltage in the 1-2 Kc range which goes to a phase detector assembly for comparison with a 1-1.9 Kc frequency-precise voltage from loop 1 of CLL-1. The reactance tube synchronizes the system so that the 510-519.9 Kc output at jack V703 is proper for reception by the high frequency group CHG.

A fourth feature of the CLL is a test oscilloscope to monitor the products of phase detectors in the L1, L2, and L3 loops.

4-7. Primary Standard Model CSS-1 (Part of SBG-1) Figure II - 4-10.

The heart of the CSS-1 is a precision oscillator within an oven containing transistors, zenner diodes to control heating, and other elements. The oscillator has a stability per day of one part in 10^8. Parallel 1 mc transistor amplifiers Q601, Q602 amplify the oscillator's 1 mc output, which is passed on to 1 mc output terminals J601, J602, and J606.

The primary standard contains a phase detector network in order to compare the precision oscillator's output with either a primary standard, such as exists in Washington, or an external 1 mc source of voltage. The 25-0=25 microammeter M601 is used as a standard of frequency comparison. Schematic, figure II - 4-6, elaborates on the technical details indicated on block diagram, figure II - 4-10.

4-8. Divider Chain Model CHL-1 (Part of SBG-1) Figure II - 4-11.

Refer to paragraph 4-1.d in this part of the manual for the role played by phantastron dely circuits V104, V105, V107 and V108. V102 is a usual type 2:1 delay multivibrator.

The time constants on which the multivibrators largely depend for their frequency-dividing action as follows :

Multivibrator	Time Constants
V102	C101, R103
V104	C109, R155, p/o R144
V105	C134, R156, p/o R124
V107	C120, R137, p/o R135
V108	C126, R148, p/o R147

The Frequency-dividing action of the multivibrators also are a function of other parameters such as stray capacitances (important at their higher frequencies), cathode bias, triggering time, etc. At the lower frequencies, hwoever , note that the product CR largely controls the frequency-dividing action of the multivibrators.

V108	1000:100	Delay 10,000 Ms	C-5000,R-2.2 Cr-110,00Mc
V107	10,000:1000	Delay 1000 Ms	C-560, R-2.2 CR-1230 Ms
V105	100,000:10,000	Delay 100 Ms	C-56, R-2.2 CR-123 Ms

Shhematic, figure II - 4-7, elaborates on the technical details indicated on block diagram, figure II - 4-11.

4-9. Power Supply, Model CPP-2 (Part of SBG-1) Figure II - 4-12.

The CPP-2 provides:

a. +380 volt unregulated power supply.

b. -400 volt unregulated power supply.

c. +160 volt regulated power supply.

d. +75 volt regulated power supply.

e. -6 volt regulated power supply.

f. 6.3(AC) volt regulated power supply.

These supplies are routed as follows:

a. Item a above, to CLL (J501,8) and to CMO(J502, 8/9).

b. Item b above, to CLL(J501, 5).

c. Items c above, to CLL (J501, 16) to CMO(J502, 16), and to CHL (J503, 16).

d. Items d above, to CLL (J501,4).

e. Item e above, toe CHG(J503, 1), to CMO (J502,1) and to CL L (J503,9).

f. Item f above, to CHG (J503, 13/15), to CMO (J503, 13/15) and to CLL (J503, 13/15).

T502 is a regulated 50/60 cycles transformmer. Two secondary positions, one for 60-cycle supply and one for 50-cycle supply are indicatd. T502 is arranged for 115/230-volt supply. Schematic, figure II - 4-8, elaborates on the technical details indicated on block diagram figure II - 4-12.

PART III

TONE INTELLIGENCE SYSTEM (TIS-3)

Section 1

General Description

III - 1-1. Introduction

III - 1-2. Functional Description of TIS-3 Unit

III - 1-3. Reference Data

Section III

Operator's Section

Section 4

Principles of Operation

III-4-1. General.

As shown by functional block diagram figure III - 4-1, the TIS-3 accepts three types of d-c signals (FSK, CW, FAX) and converts them into audio frequency output signals for sideband transmission via an associated SBG-1 unit thatprovides its RF sideband transmitter with the required RF intelligence.

The Key-line (FSK, CW) input is fed to an isolation keyer, which is also supplied by an 198.10 or 198.00 or 197.45 Kc crystal oscillator output. The first stage of the isolation keyer has an output of spurts of the crystal oscillator's input, as controlled by the key-line signal (which make a pair of diodes successively conducting and non-conducting). A second group of diodes rectify the spurts of IF. The keyer V3, V4B prepares the RSK signals to "frequency shift" the 200 kc oscillator which is equipped with a reactance tube. The FAX isolation tube V6B also frequency shifts V1, V2. The frequency-shifted 200 kc FSK, FAX signals proceed to mixer V5 where they are heterodyned with crystal oscillators 198.10 or 198.00 of 197.45 Kc output. The output of mixer V5 consists of frequency shifted 1900 cps or 2000 cps or 2550 cps FSK, FAX signals which are amplified in audio amplifier V7 and then proceed to the associated SBG-1 CBE-1's audio input, channels 1 or 2.

On CW signals, keyer V3, V4B output is amplified by V4A to provide cathode bias to audio amplifier V7. Mixer V7's output consists of 1 Kc spurts that again are routed to the associated SBG-1 CBE-1's audio input, channels 1 OR 2.

For a stage-by-stage description of the TIS-3 see following paragraphs III - 4-2 through III - 4-7 in conjunction with simplified schematics III - 4-2 through - III - 4-7 and overall schematic diagram III - 8-1.

III - 4-2. Crystal Oscillator V 8 (Figure III - 4-2.)

III - 4-3. Isolation Keyer (Figure III - 4-3.

III - 4-4. Keyer V3, V4 (Figuee III - 4-4.

III - 4-5. 200 Kc Oscillator/Reactance Tube V1, V2(Fugure III - 4-5).

III - 4-6. FAX Isolation Tube V6B(Figure III - 4-6.

III - 4-7. Mixer (V5) CW Oscillator (V6A) and Audio Amplifier (V7) (Figure III - 4-7).

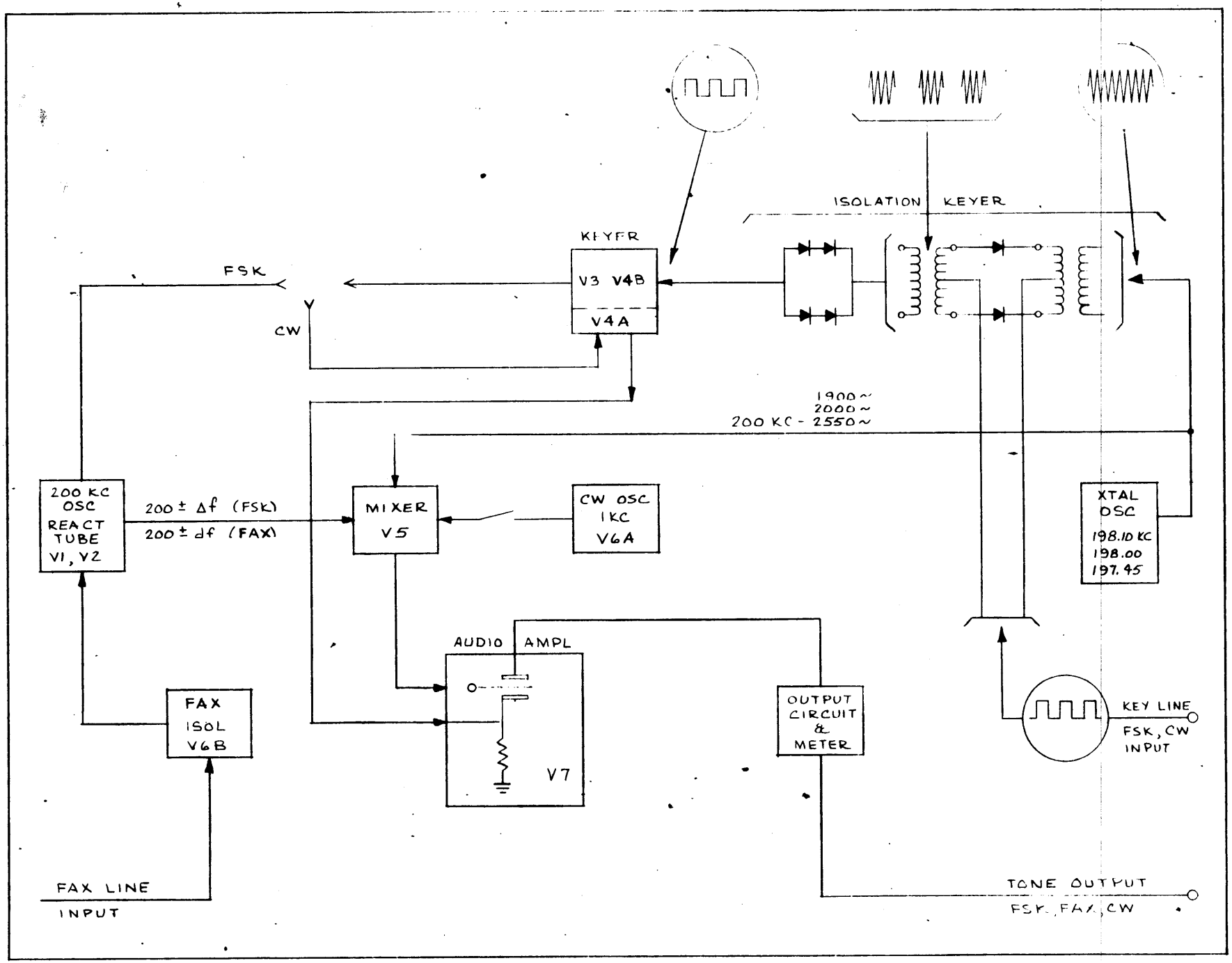


FIGURE III-4-1 FUNCTIONAL BLOCK DIAGRAM OF TONE INTELLIGENCE SYSTEM MODEL TIS-3 (A COMPONENT OF SBG-1)

FIGURE III-4-1 (CK-464
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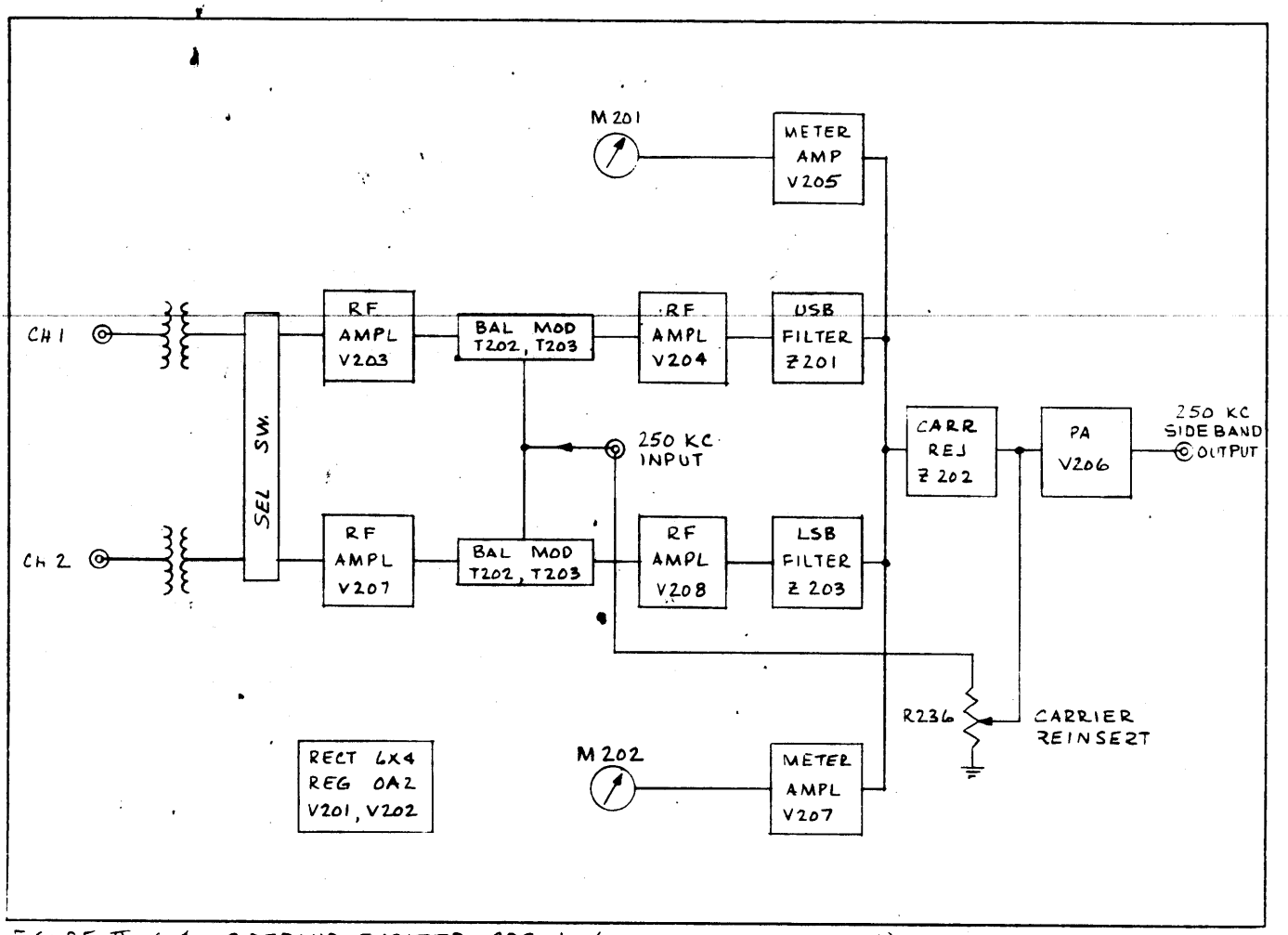


FIGURE II-4-4 SIDEBAND EXCITER, CBE-1 (COMPONENT OF SBG-1)

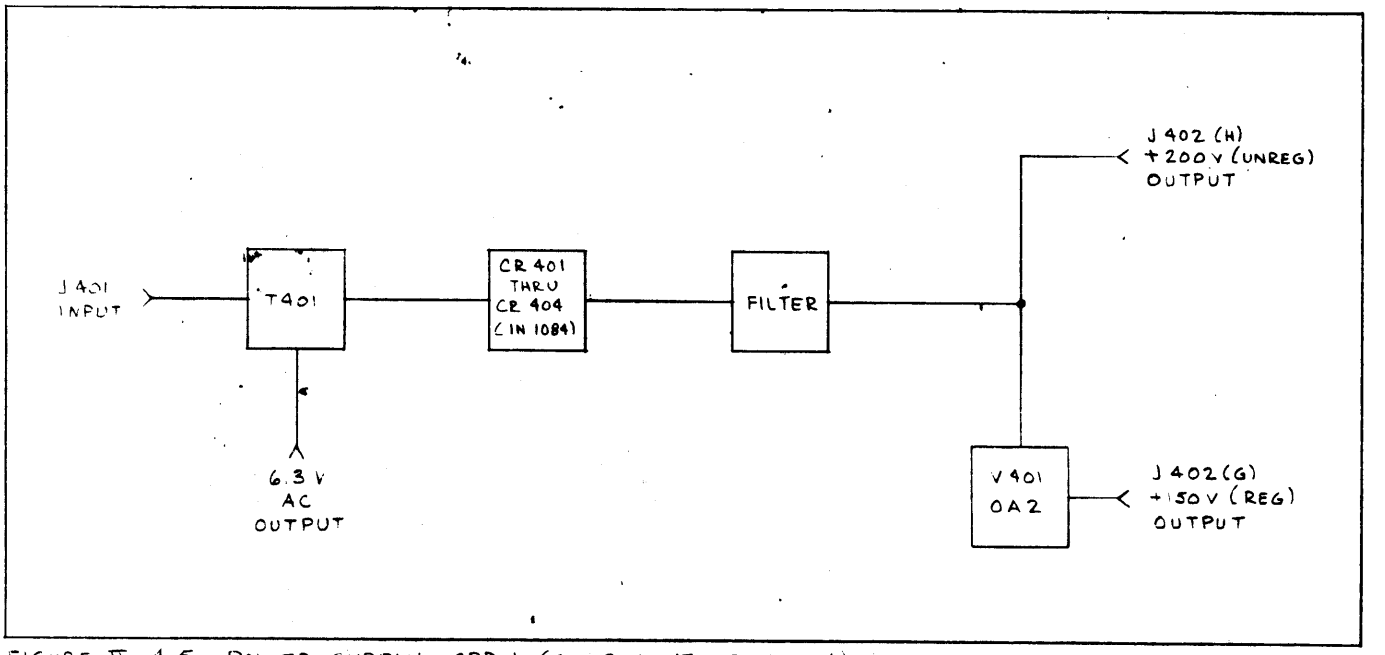
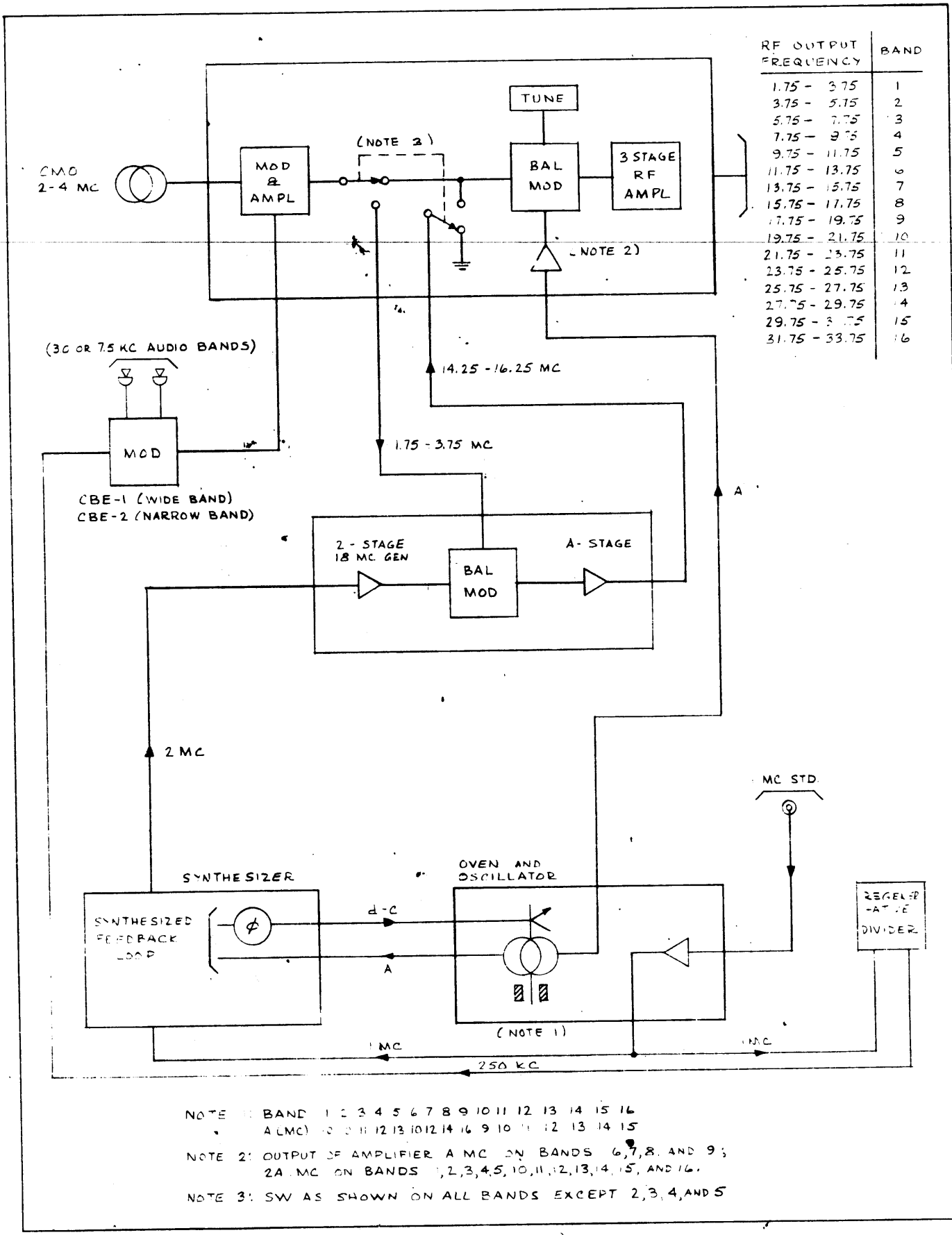


FIGURE II-4-5 POWER SUPPLY, CPP-1 (COMPONENT OF SBG-1)

FIGURE II-4-4 (CK-445)
FIGURE II-4-5 (CK-450)



RF OUTPUT FREQUENCY	BAND
1.75 - 3.75	1
3.75 - 5.75	2
5.75 - 7.75	3
7.75 - 9.75	4
9.75 - 11.75	5
11.75 - 13.75	6
13.75 - 15.75	7
15.75 - 17.75	8
17.75 - 19.75	9
19.75 - 21.75	10
21.75 - 23.75	11
23.75 - 25.75	12
25.75 - 27.75	13
27.75 - 29.75	14
29.75 - 31.75	15
31.75 - 33.75	16

NOTE 1: BAND 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
A (MC) 2 3 11 12 13 10 12 14 16 9 10 11 12 13 14 15

NOTE 2: OUTPUT OF AMPLIFIER A MC ON BANDS 6, 7, 8, AND 9;
2A MC ON BANDS 1, 2, 3, 4, 5, 10, 11, 12, 13, 14, 15, AND 16.

NOTE 3: SW AS SHOWN ON ALL BANDS EXCEPT 2, 3, 4, AND 5

FIGURE II-4-6 AMPLIFIER, CHG-1 (COMPONENT OF SBG-1)

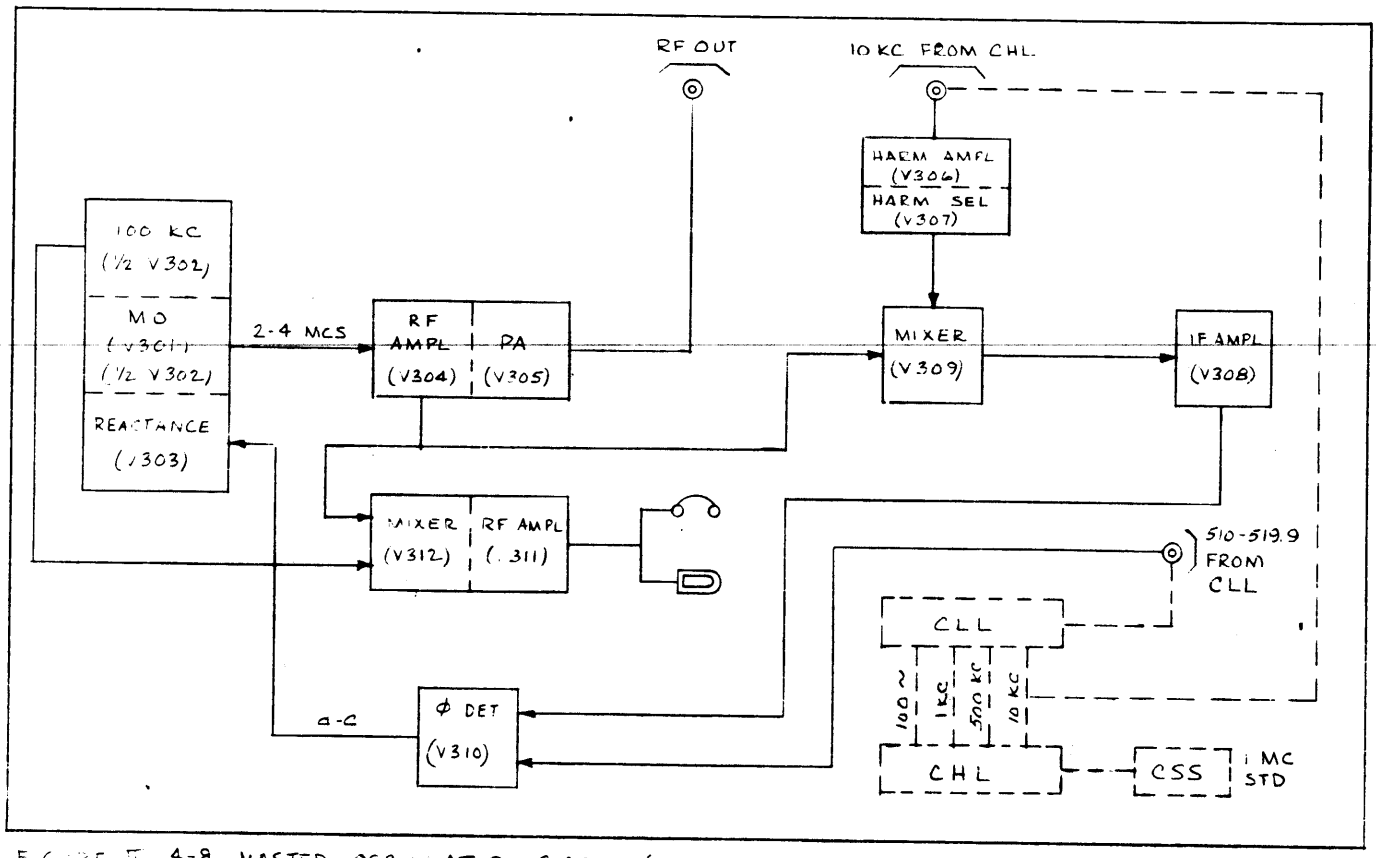
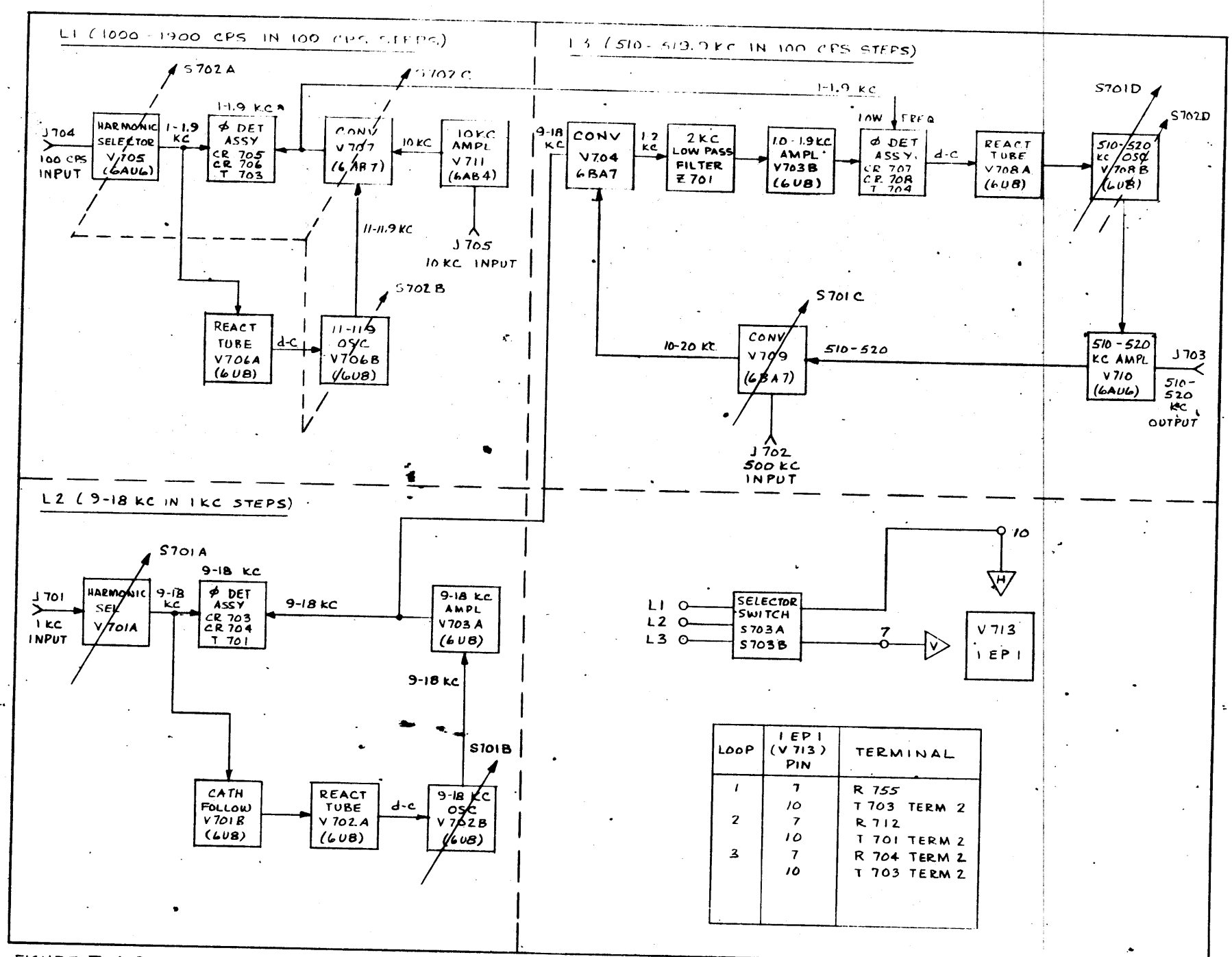


FIGURE II 4-8 MASTER OSCILLATOR, CMO-1 (COMPONENT OF SBG-1)

FIGURE II 4-8 (CK-439)



LOOP	1 EP 1 (V 713) PIN	TERMINAL
1	7	R 755
	10	T 703 TERM 2
2	7	R 712
	10	T 701 TERM 2
3	7	R 704 TERM 2
	10	T 703 TERM 2

FIGURE II-4-9 LOW FREQUENCY LOOP, CLL-1 (COMPONENT OF SBG-1)

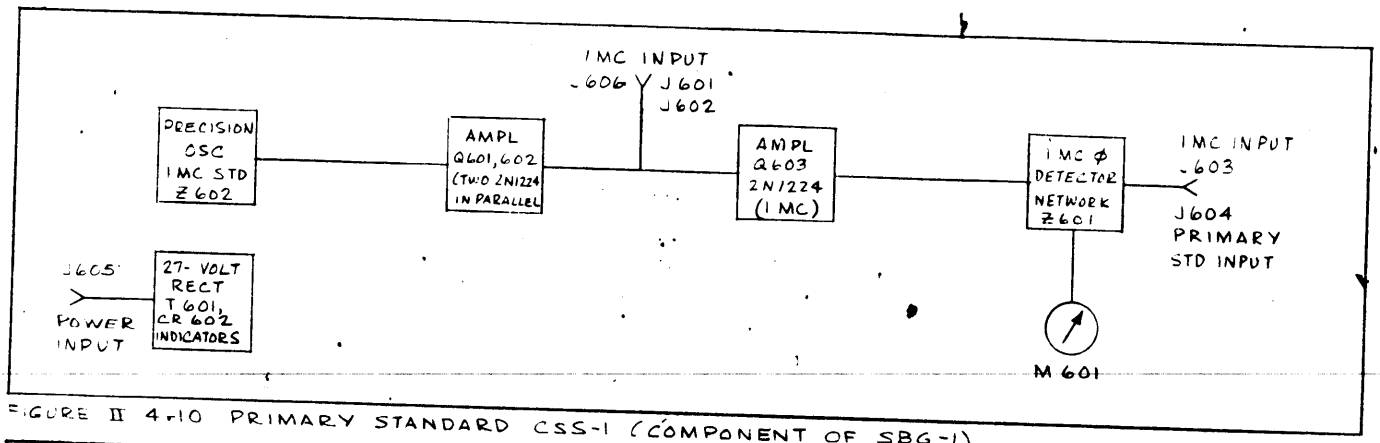


FIGURE II 4-10 PRIMARY STANDARD CSS-1 (COMPONENT OF SBG-1)

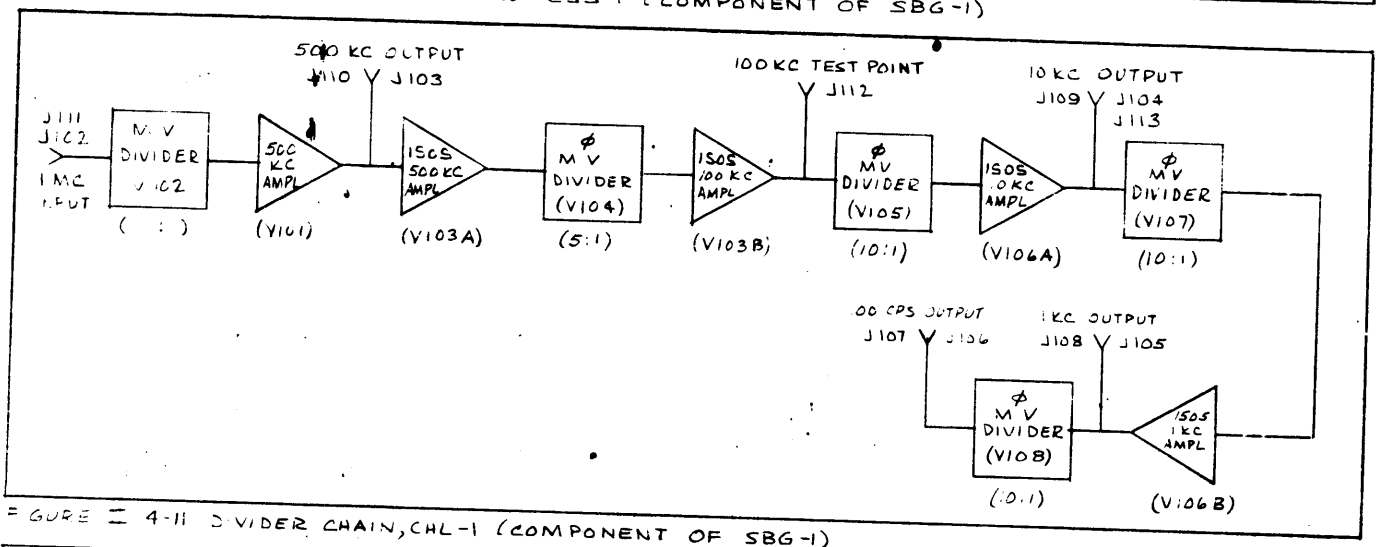


FIGURE II 4-11 DIVIDER CHAIN, CHL-1 (COMPONENT OF SBG-1)

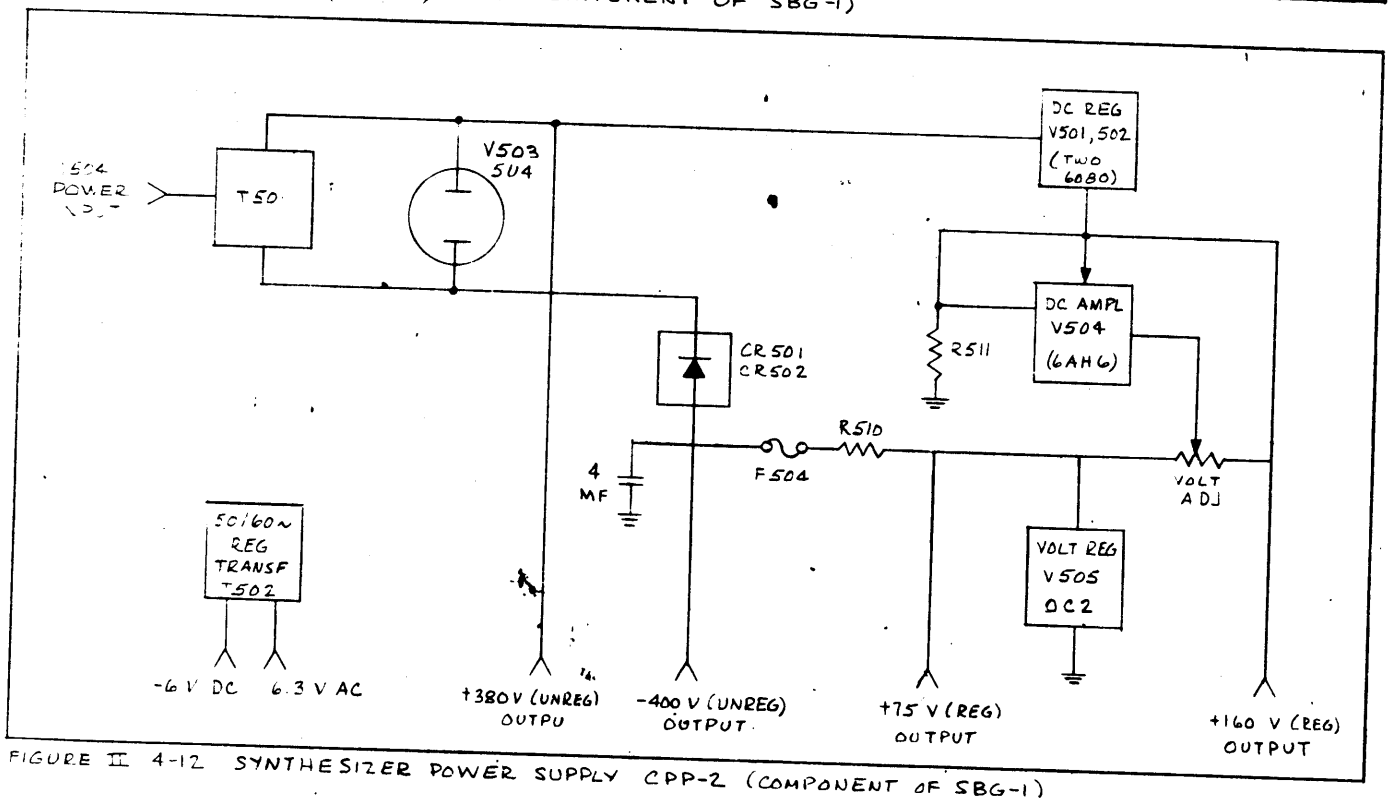


FIGURE II 4-12 SYNTHESIZER POWER SUPPLY CPP-2 (COMPONENT OF SBG-1)

FIGURE II 4-10 (CK-441)
FIGURE II 4-11 (CK-386)
FIGURE II 4-12 (CK-440)

MJT 1-16-61

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COMPLETE TEST INSTRUCTIONS

FOR

THE SBG SYSTEM

DATE 12/28/60
SH. 2 OF 11
COMPILED BY
A.R.F.

TMC SPECIFICATION NO. S

TITLE: TESTING OF THE SBG SYSTEM

JOB

APPROVED A.R.F.

I. Preliminary

A. Connect RF and power cables to units as shown in CK-468.

B. Inspect rack for mechanical imperfections.
   1. Insure that cables are free when separate units are pulled out and tilted from rack.
   2. Units should line up in rack together; there should not be any contact between front panel edges.
   3. Units should slide freely.

C. Connect power to rack input J909.

D. Set CPP-2 and CHG Power switches to "ON". CHG and CMO over lights should be on. Because of the delay tube in the CPP-2, a 60 second wait is necessary before B+ is applied to its associated units. This should be observed.

E. CBE and CSS power switches should be turned to their "ON" positions.

F. SBG system should have at least a 24 hour warm-up period before testing. This will allow ovens to warm-up and cycle.

II. Test Equipment Required

A. 1 70 ohm, non inductive, 5 watt resistance.

B. 1 electronic counter, H.P. 524C or equivalent.

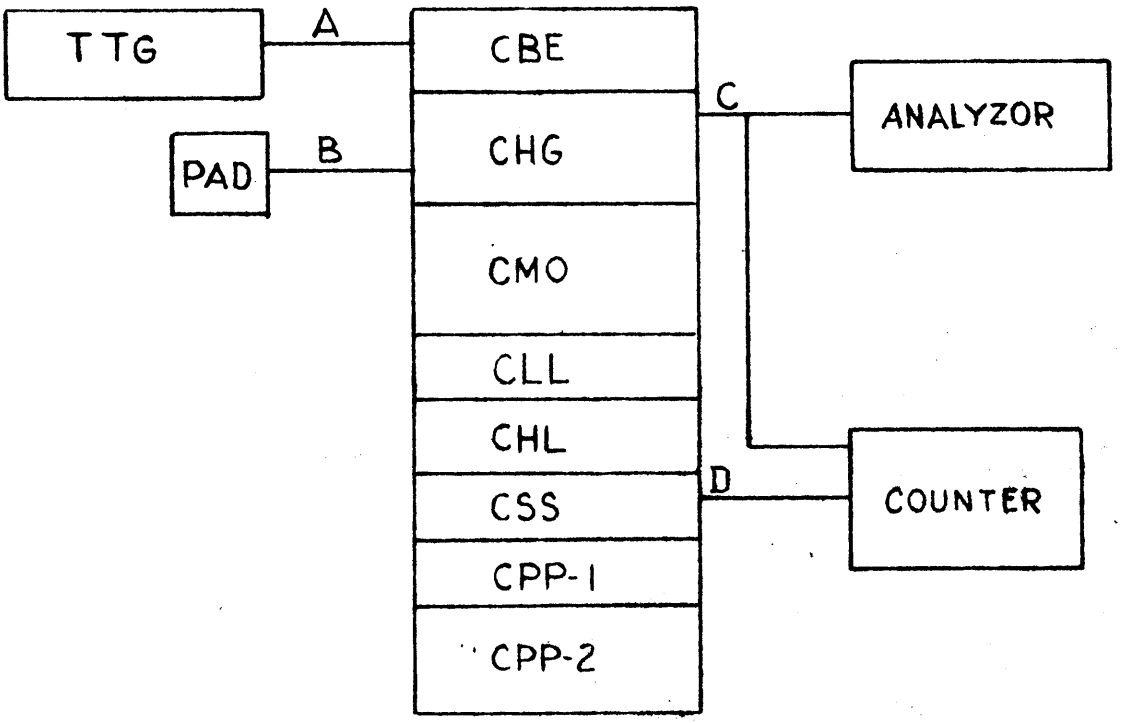
C. 1 RF VTVM, H.P. 410B or equivalent.

D. 1 Panaramic analyzor Model SB-12A.

E. 1 Model TTG, two-tone generator or equivalent.

FIGURE 1

TEST EQUIPMENT SET-UP



A. Two-tone audio from TTG to channel 1 or channel 2 of the CBE. A single conductor shielded wire can be used for this purpose. TTG connections are as follows: Shield of wire to terminal 2 of E 500, audio out strip. Insulated wire should be connected to terminal 1 of E 500. The remaining end of the shielded wire should be connected to the CBE in the following manner. For channel 1, connect shield of wire to terminals 1 and 2 of E 201. Insulated wire should be connected to terminal 4. For channel 2, connect shield of wire to terminals 8 and 9. Insulated wire should be connected to terminal 6.

Either one of the two channels can be used. A check should be made, with the channel that is not going to be used throughout the complete frequency test, with at least one of the test frequencies. This is to insure that the channel is functioning properly, and the chann l switch is wired prop rly.

B. CHG J-1104 output connected to load.

C. CHG J-1105 monitor connected to analyzor and counter signal input connectors.

D. CSS J-1602 IMC out to counter frequency standard input; set counter standard switch to external. This is to eliminate any error in the output frequency readout on the counter due to a difference in frequency between the SBG standard (CSS) and the standard in the count r.

III. GENERAL CHECK-OUT

This can only be accomplished by the completion of a 24 hour warm-up.

A. Observe if ovens are cycling in CMO and CHG (i.e. oven lights should go on and off).

B. The CMO drive control should be turned approximately mid-range. This is to prevent pinning the CHG MF meter.

C. A square should appear on the scope in the L-1, L-2, and L-3 positions of the CLL. This should be true for all the positions on the KCS and CPS switches.

D. The CHG sync indicator light should remain on in each of the band switch positions.

E. Connect test equipment as shown in figure 1.

F. Set CMO counter dial to 1750 KCS, function switch in calibrate position. Beat should be observed on calibrate indicator light. If not, alignment of the osciliator ends is necessary.

1. OSCILLATOR ALIGNMENT

a. Set CMO counter to 1750 KCS. 1750 KCS should be approached from the lower frequency side (i.e. 1650 KCS to 1750 KCS). This will prev nt any error due to backlash.

b. Rotate calibrate knob until beat on calibrate indicator light is observed. As an additional check, the output of the CMO through a 20 db pad, can be read on the counter.

c. Set CMO counter to 3750 KCS. Again, as in the 1750 KCS cas , 3750 KCS should be approached from th lower frequency sid (i.e. 3650 KCS to 3750 KCS).

d. Rotat MO "High End" trimmer until beat on

111. cont'd.

calibrate indicator light is observed. This trimmer is located behind the front panel hole adjacent to the calibrate knob.

e. Repeat step a. through d. until beat is observed at 1750 KCS and 3750 KCS without further adjustments. This completes the oscillator alignm nt.

G. Output of the TTG should be adjusted to .015 volts at the terminals of the CBE.

H. Set CBE channel switches to 1 or 2, depending on terminal connections. Carrier control to "OFF" position; TTG set for two tones audio.

1V. SBG TUNING

A. DETERMINING OUTPUT FREQUENCY

The output frequency is determined by adding the bandswitch numeral which is in MCS, to the CMO output frequency. Take for example, that a frequency of 12,751,200 cycles is desired. Bandswitch is set to 11.750-13.750, number 10 position.

10,000,000 cycles + 2,751,200 cycles=12,751,200 cycles.

B. CMO AND CLL ADJUSTMENT

1. Turn CMO function switch to operate and MO counter to 2750 KCS.
2. Vary Tuning KCS control for maximum reading on output tune meter. This will occur at approximately 2.75 on the panel dial.
3. The KCS switch is set to (1) one, and the CPS switch at (2) two. This is because the synthesizer only controls the 100 cps and 1000 cps digits of the MO. We depend on the MO accuracy for the thousand, hundred, and ten digits on the MO counter. Note the color coding and CLL and CMO panels.
4. Synchronizing of CMO at 2750 KCS.
   a. Vary the MO control approximately 2 KC above and below 2750 KCS. The sync meter will follow in the same direction as this control is varied (i.e. when the MO control is varied to the right the sync meter pointer will move to the right). At the same time the sync indicator will ignit .
   b. Vary the MO control 1KC abov and b low 2750KCS (i.e. 2751KCS-2749KCS). Th sync indicator light should r main on. The sync meter should follow the variation of th MO control through the gr n rang of th sync meter fac . This is regard d as the lock-in range.

IV. cont'd.

c. As a final check on sync action, vary the MO control slowly approximately 3 KCS above and below 2750 KCS. As the loop drops out of sync, (sync meter will fall to center scale position) the sync indicator light will go off.

C. CHG ADJUSTMENT

1. Bandswitch is set to the output frequency desired. In the case of the example, it is set at 11.750-13.750, Band Switch No. (10) ten.
2. Vary the MF tuning control for maximum indication on the CHG MF tuning meter. Care should be taken as in Part III B. This will occur at approximat ly 2.75 on the panel dial in the example. MF tuning meter must never be operated in the red region.
3. Turn B+ switch to "ON" position.
4. Peak output meter at 1750 KCS with the main tuning control.
5. Rotate output control to on output meter reading of approximately 8 or 9.
6. The counter will read the the output frequency $\pm$ one count. In the case of the example it will read 12,751,200 cycles.
7. Set up frequencies 25,200, 400 cycles and 30,800, 900 cycles. Note the read out on the counter. It can be seen in the Test Equipment set-up, figure 1, that the CSS is also used as the standard for the counter. Therefore, any error in the counter read-out is due to the CSS IMC STANDARD.
8. With the output control fully clockwise, the output voltage across the 70 ohm load should be 8.5 volts or better.

V. DISTORTION TEST

A. Panalyzor adjustment for measuring distortion.

1. Gain- full clockwise position.
2. Amplitude scale switch-LOG.
3. Cal. OSC level-OFF.
4. Input Attenuators-OFF.
5. I. F. Att nuation-20 db.
6. Sweep width selector-10KC.
7. AFC-OFF.

V. cont'd.

8. The VOX should be set at 500KC above the frequency being measured. In the case of the example, 12, 751,200 cycles, the VOX frequency should be set at approximately 13,251,200 cycles.

B. Distortion measurements should be taken at the frequencies indicated on Chart 1. In each case, the distortion products must be at least 40db down on two tone test.

VI. SPURIOUS

A. Set CBE channels to "OFF". Carrier should be inserted to maximum of (0) zero position.

B. Analyzor sweep should be set on 500 cycles.

C. Distortion measurements should be taken at the frequencies indicated on Chart 1. In each case, spurious should be down 60db or better.

D. It is important that the spurious check should be made through the complete lock-in range of the CMO.

VII. CARRIER SUPPRESSION

A. Set analyzor IF attenuator to the 20db position.

B. With the carrier adjusted as above, set the carri r represention on the analyzor screen to the (0) zero DB line.

C. Swith IF attenuator to (0) zero db position.

D. Rotate carrier control to OFF position.

E. Carrier should be down 55 db or better.

VIII. SIDE BAND CHECK

A. Set carrier to OFF position.

B. TTG AUDIO TONE SELECTOR set to TONE 1 position.

C. Set CBE USB switch to channel 1 or 2 depending on terminal connections to E201, LSB Switch to OFF.

D. Read frequency on counter.

E. Set CBE LSB switch to channel 1 or 2 depending on terminal connections to E201, USB switch to OFF.

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VIII. cont'd.

F. Read frequency on counter. This frequency should be 1870 CPS lower than first reading if a 935 CPS tone is used from the TTG. If this second reading is not lower in frequency, check for proper filter plac ment in the CBE or cable connections.

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CHART 1

TEST FREQUENCIES			Band SW. NO.	Output tuning Dial Band
1.750	2.750	3.750	0	A
3.750	4.750	5.750	2	B
	4.000		2	B
	5.000		2	B
5.750	6.750	7.750	4	C
7.750	8.750	9.750	6	C
9.750	10.750	11.750	8	C
11.750	12.750	13.750	10	C
13.750	14.750	15.750	12	D
15.750	16.750	17.750	14	D
17.750	18.750	19.750	16	D
19.750	20.750	21.750	18	D
21.750	22.750	23.750	20	D
23.750	24.750	25.750	22	D
25.750	26.750	27.750	24	D
27.750	28.750	29.750	26	D
29.750	30.750	31.750	28	D
31.750	32.750	33.750	30	D

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TEST REPORT SHEET

A. Mechanical

1. Slides_____

2. Front panel line-up_____

3. Cables_____

B. Oven cycling

1. CMO_____

2. CHG_____

C. CMO

1. Calibration_____

2. Beat Indicator_____

D. CHG

1. Output voltage_____

E. Carrier Suppression_____DB

Lower Band Limit		Upper Band Limit	Band Sw Number	Output Tuning Dial Band	Counter	Spurious	Distortion
1.750	2.750	3.750	0	A			
3.750	4.750	5.750	2	B			
	4.000		2	B			
	5.000		2	B			
5.750	6.750	7.750	4	C			
7.750	8.750	9.750	6	C			
9.750	10.750	11.750	8	C			
11.750	12.750	13.750	10	C			
13.750	14.750	15.750	12	D			
15.750	16.750	17.750	14	D			
17.750	18.750	19.750	16	D			
19.750	20.750	21.750	18	D			
21.750	22.750	23.750	20	D			
23.750	24.750	25.750	22	D			
25.750	26.750	27.750	24	D			
27.750	28.750	29.750	26	D			
29.750	30.750	31.750	28	D			
31.750	32.750	33.750	30	D			

Serial Number_____

Date_____

Tested by_____

Accepted by_____

APPROVED

COMPILED BY A. R. F.

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