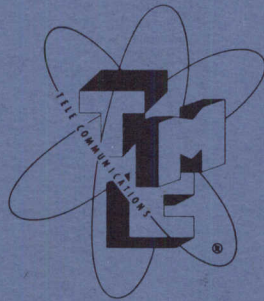


TMC Synthesizer

Andrew Baczynsky



THE TECHNICAL MATERIEL CORP.

Mamaroneck, N. Y.

Ottawa, Ontario



FINAL REPORT

ON

Technical Materiel Corporation  
Portable Master Oscillator Control Synthesizer

DEVELOPED BY

Electronics Research Laboratory  
Montana State College  
Bozeman, Montana

Report prepared by William E. Beale  
Research Assistant

SPECIFICATIONS

The P.M.O. Control Synthesizer, developed for use with TMC's Portable Master Oscillator, controls the oscillator frequency in exact 100-cycle steps from 2 to 4 MC. The accuracy of the system is controlled by an external 1 MC standard.

INPUT SIGNAL REQUIREMENTS

A 1 MC standard, of the desired stability and accuracy, furnishing 1 volt in 50 ohms.

INPUT POWER REQUIREMENTS

Plate Supply: +200 volts at 280 MA regulated.

Filament Supply: 6.3 volts at 9.5 amp. regulated. SOLA  
6.3 volts at 5.4 amp. unregulated.

Bias Supply: -150 volts at 30 MA regulated.

OUTPUT SPECIFICATIONS (at 3 MC output frequency)

Spurious Signals: \* 10 kc from desired, 130 db down  
‡ 510 kc from desired, 90 db down  
‡ 60 cps, from desired, 40 db down

## THEORY OF OPERATION

### General

The frequency synthesizer controls the frequency of the TMC portable master oscillator, P.M.O., in 100 cps steps from 2 to 4 MC. These controlled frequencies are synthesized from a 1 MC standard such that the accuracy and stability of the system is exactly that of the standard. The synthesizer is composed of a high frequency deck and a low frequency deck which are controlled by the divider chain.

The calibration accuracy of the P.M.O. is such that the synthesizer need only control the 100 and 1000 cps digits.

The high frequency deck converts the P.M.O. output frequency to an intermediate frequency of 510 to 520 kc. The low frequency deck provides an output of 510 to 520 kc in 100-cycle steps for comparison with this intermediate frequency. These two frequencies are compared and a dc voltage derived which controls the P.M.O.

### Divider Chain

The divider chain receives the standard 1 MC input and furnishes 100, 1,000, 10,000, and 500,000 cps output frequencies for the low and high frequency decks.

### High Frequency Deck

The high frequency deck develops a 510 to 520 kc signal to be compared with the output of the low frequency deck. The 10 kc from the divider chain is used to trigger a pulse generator. This pulse generates harmonics of 10 kc from 1.49 to 3.49 MC. A selected harmonic is mixed with the output of the P.M.O. to yield the desired comparison signal.

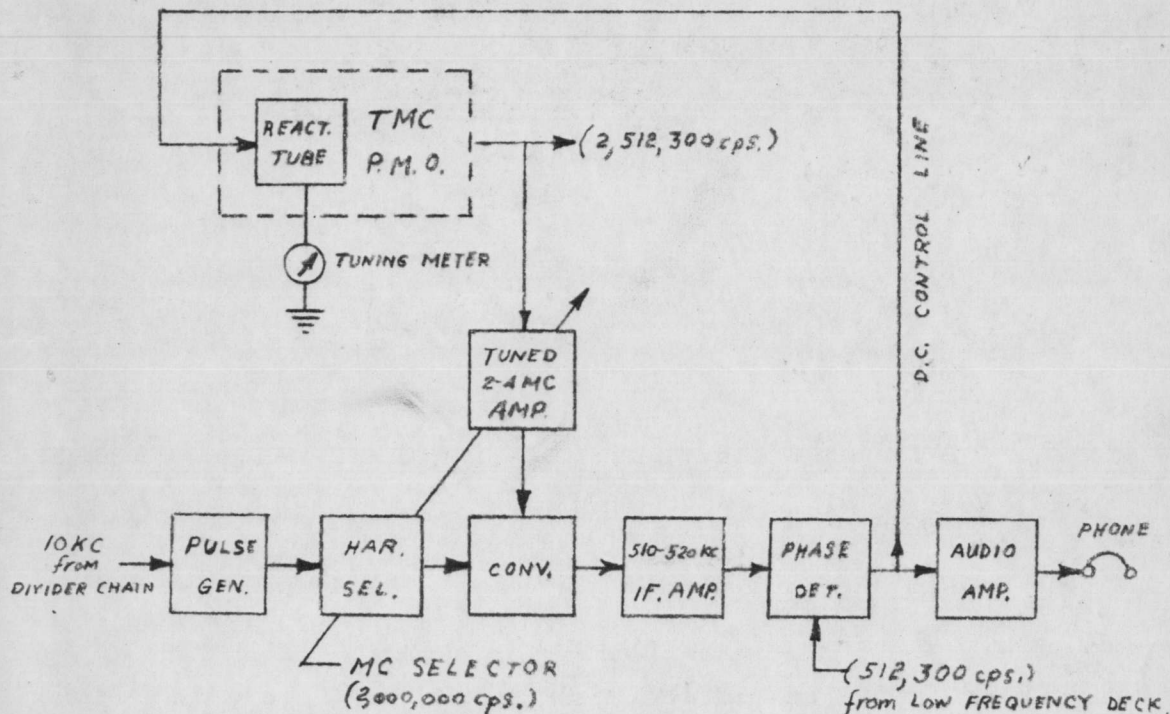
The high frequency deck is analogous to a superheterodyne receiver. The harmonics of the 10 kc pulse simulate the broadcast stations and the P.M.O. simulates the local oscillator.

A tuned amplifier on the output of the P.M.O. is ganged to the harmonic selector. Therefore, when the amplifier is tuned to the P.M.O. output frequency, the correct harmonic 510 kc below the P.M.O. frequency is selected. The selected harmonic frequency and the P.M.O. frequency are mixed in a converter, and the resultant difference frequency is selected and amplified by an IF amplifier. This output is compared in a phase detector with the output of the low frequency deck.

The dc voltage output of the phase detector is applied to the reactance tube in the P.M.O. and synchronizes the P.M.O. to the low frequency deck.



The following block diagram and numerical example should clarify the operation of the high frequency loop.



Assume that the desired frequency of the P.M.O. is 2,512,300 cps. This implies that the output from the low frequency deck be 512,300 cps, the 100 and 1000-cycle digits being selected by this frequency. The P.M.O. will be tuned to about 2,510 kc selecting the tenth, hundredth, and thousandth kc digits. The 2 to 4 MC amplifier will then be tuned to a maximum causing the ganged harmonic selector to select the 2,000 kc harmonic frequency. The IF frequency will then be approximately 510 kc. Since this IF frequency is not equal to the 512.3 kc furnished by the low frequency deck, the output of the high frequency phase detector will be an audio difference frequency.

This audio is amplified and monitored by the operator through the audio amplifier and phones. Since the amplitude of this audio tone is a direct function of the amplitude of the harmonic being selected, readjustment of the MC tuning for maximum amplitude of tone will eliminate any tracking error that may exist between the 2 to 4 MC amplifier and the harmonic selector.

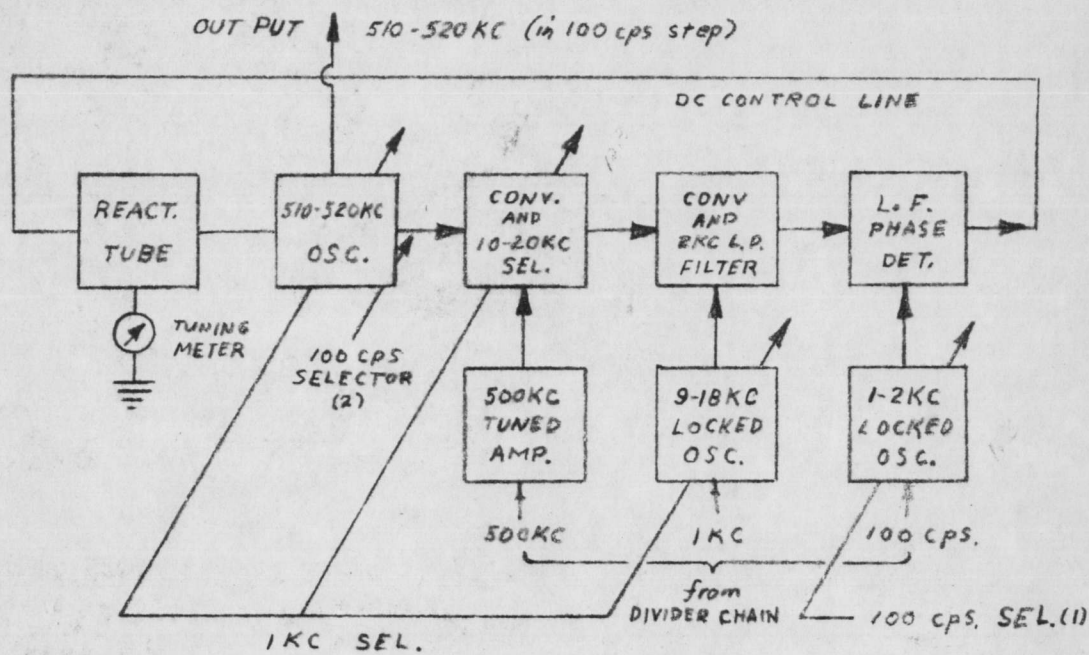
The P.M.O. tuning then is adjusted for zero beat note in the phones and the system will synchronize. A tuning meter in the cathode circuit of the reactance tube gives a direct indication of the dc control voltage being developed when the system is synchronized.

Since the system is synchronized this indicates that the IF frequency must be 512.3 kc hence the output frequency is the desired 2,512,300 cps.

Low Frequency Deck

The low frequency deck furnishes an output of 510 to 520 kc settable in 100-cycle steps. This output is generated by a synchronized oscillator which is referenced by a series of conversions to the 100 and 1000 cps outputs of the divider chain.

The following simplified block diagram of the low frequency deck will illustrate the operation.



The output frequency is controlled by the kc selector and two 100-cycle selector switches. The kc selector steps the frequency of the 510 to 520 kc oscillator, the 10 to 20 kc selector, and the 9 to 18 kc locked oscillator in 1 kc increments. The 100-cycle selector (1) determines the frequency of the 1 to 2 kc locked oscillator in 100-cycle steps and the 100-cycle selector (2) varies the 510 to 520 kc oscillator frequency between the kc settings.

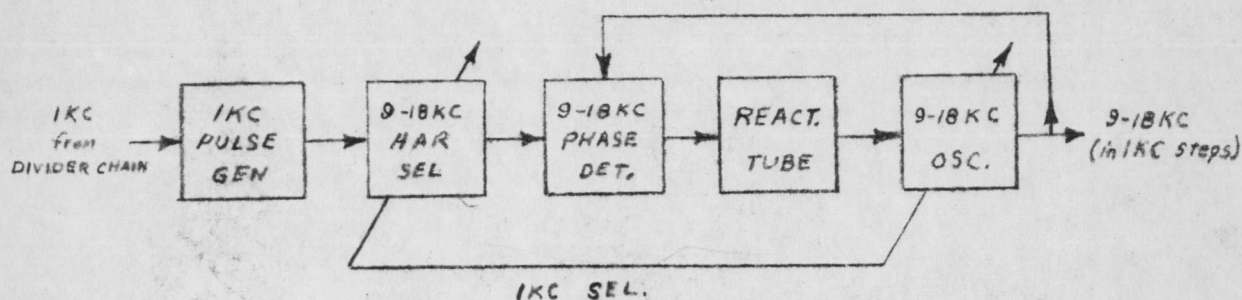
The 510 to 520 kc oscillator frequency is converted to 1 to 2 kc. This 1 to 2 kc is compared with the output frequency of the 1 to 2 kc locked oscillator in the low frequency phase detector. The 100-cycle selector (2) is adjusted until these two frequencies are equal. The output of the phase detector will be a dc voltage and the system will be synchronized. Synchronism will be evidenced by a variation in the tuning meter as a slight adjustment of the 100 cycle selector (2) is made.



As a numerical example, assume that the 2 kc and 300-cycle positions of the selectors are chosen. This will produce an output frequency of 512,300 cps. The 2 kc selection positions the oscillator at 512 kc, the 10 to 20 kc selector at 12.5 kc and the 9-18 kc locked oscillator at 11 kc. The 100-cycle selector (1) in the 300 cps position sets the 1 to 2 kc locked oscillator at 1.3 kc and the 100-cycle selector (2) repositions the 512 kc oscillator to approximately 512,300 cps. The 100-cycle (2) is then adjusted slightly until the loop is synchronized.

The synchronization of the loop demands that the output of the deck be exactly 512,300 cps. This 512.3 kc is mixed with 500 kc, the difference frequency, 12.3 kc, being selected by the 10 to 20 kc selector. This 12.3 kc is mixed with the 11 kc output of the 9-18 kc locked oscillator producing a 1.3 kc signal to the phase detector. This 1.3 kc and the 1.3 kc from the 1 to 2 kc locked oscillator are compared in the phase detector producing the dc synchronizing voltage.

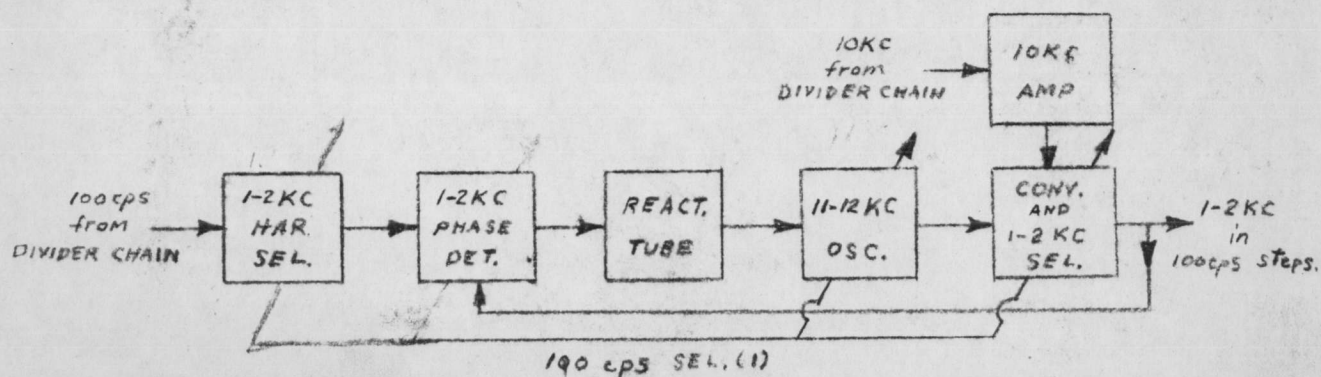
The functioning of the 9 to 18 kc locked oscillator is illustrated in the following block diagram.



An oscillator is locked on a harmonic of a 1 kc pulse. The 1 kc from the divider chain triggers a pulse generator. This pulse is rich in harmonics from 9 to 18 kc. The desired harmonic is selected and compared with the output frequency of the 9-18 kc oscillator in a phase detector. The dc output voltage of the phase detector synchronizes the oscillator to the selected harmonic.

The 1 to 2 kc locked oscillator operates in a similar manner, except that the actual frequency of the oscillator is 11 to 12 kc. The desired 1 to 2 kc is obtained by converting the 11 to 12 kc to 1 to 2 kc with 10 kc from the divider chain.

The following block diagram should clarify the operation of this loop.



GENERAL CHECKOUT PROCEDURE

The following checkout is to be made with the synthesizer and P.M.C. completely interconnected, power supplied to all units and a 1 MC (1 volt in 50 ohms) signal applied to the divider chain.

An oscilloscope, Tektronix Model 515 or equivalent, and a counter, Hewlett-Packard 523 or equivalent, will be the necessary checkout equipment.

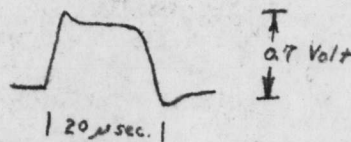
I. Divider Chain

Verify that the 500 kc, 100 kc, 10 kc, and 1 kc and 100 cps signals are correct. This may be done by monitoring the frequency on a counter connected to the corresponding test point. The 500 kc is not adjustable, but the 100 kc, 10 kc, 1 kc and 100 cps dividers may be adjusted to provide the proper output frequencies. Adjustment is made by means of a potentiometer located below and to the left of each of these test points. Note that the outputs must be connected to their loads since the capacity of the coaxial connectors influences the divider action. After the divider is properly adjusted the rest of the synthesizer may be checked out.

II. Low Frequency Loop

1. 1 kc Pulse Generator

Connect an oscilloscope to the PG-out test point. The resulting waveform should be a pulse 20 usec in width and recurring at a 1 kc rate. Adjust the Bias Adj. potentiometer until a stable repetition rate is obtained, but such that a pulse is generated only when the 1 kc input is present.



2. 1-2 kc Locked Oscillator

Connect a counter to the 1-2 kc test point. Check that the output frequency corresponding to the position of the upper CPS selector is as follows:

<u>Upper CPS Position</u>	<u>Frequency CPS</u>
000	1000
100	1100
200	1200
300	1300
400	1400
500	1500
600	1600
700	1700
800	1800
900	1900



3. 9-18 kc Locked Oscillator

Connect a counter to the 9-18 kc test point. Check that the output frequency corresponding to the position of the KCS selector is as follows:

<u>KCS Position</u>	<u>Frequency cps</u>
0	9,000
1	10,000
2	11,000
3	12,000
4	13,000
5	14,000
6	15,000
7	16,000
8	17,000
9	18,000

4. 510 to 520 kc Locked Oscillator

Connect a counter directly on the 510 to 520 kc output jack. Set both the CPS selectors to 000 position and set the KCS selector to the zero position. Synchronize the low frequency loop with the lower CPS selector. (To synchronize the loop vary the lower CPS selector slightly about the 000 position until the L.F. Tuning Indicator deflection can be controlled by this selector.) With the system synchronized the output frequency should be 510 kc. Place the KCS selector in the 2 position. The loop should resynchronize without readjusting the lower CPS selector. Check that the loop is synchronized and that the correct output frequency is obtained for each of the KCS selector positions. The output frequency corresponding to each kc position with the CPS selector set at zero and with the loop synchronized should be as follows:

<u>KCS Position</u>	<u>Output Frequency cps</u>
0	510,000
1	511,000
2	512,000
3	513,000
4	514,000
5	515,000
6	516,000
7	517,000
8	518,000
9	519,000

Reset the KCS selector at 0, the CPS selectors to 100 and synchronize the loop. The output frequency should be 510.1 kc. Repeat this synchronizing procedure for each position of the CPS selector, the output frequency corresponding to each position follows:

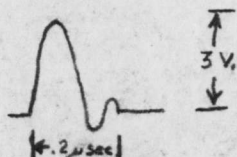
<u>CPS Position</u>	<u>Output Frequency CPS</u>
000	510,000
100	510,100
200	510,200
300	510,300
400	510,400
500	510,500
600	510,600
700	510,700
800	510,800
900	510,900

This completes the checkout of the low frequency loop.

### III. High Frequency Loop

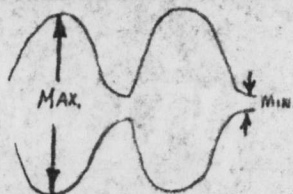
#### 1. 10 kc Pulse Generator

Connect an oscilloscope to test point, Pulse Out. Adjust the Bias Adj. until a pulse 0.2 usec in width and recurring at a stable 10 kc rate is observed. Correct bias adjustment will allow a pulse to be generated only when the circuit is triggered by the 10 kc input signal.



#### 2. 510 to 520 kc IF

Connect an oscilloscope to the IF Out test point. The following envelope pattern should be observed.



Max. (Approx.) 4.5 Volts Pk. to Pk.  
 Min. (Approx.) 1.5 Volts Pk. to Pk.  
 (At 3 MC)

3. Depress the Push to Tune switch and tune the MCS selector, for maximum on the HF Tuning indicator. Release the Push to Tune and retune the MCS selector for maximum volume in the phones. Synchronize the high frequency loop. (This is done by adjusting the P.M.O. tuning knob for a zero beat-note in the phones.) Vary the P.M.O. tuning, while observing the HF Tuning Indicator. The system should be capable of varying the indicator beyond the sync limits on the meter panel before dropping out of synchronism.



GENERAL OPERATING INSTRUCTIONS

I. FRONT PANEL CONTROLS

1. P.M.O.: Controlled - Normal

In the normal position of this switch the P.M.O. functions, independently of the synthesizer, as a variable frequency oscillator. In the controlled position the output frequency of the P.M.O. will be determined by the synthesizer.

2. Push to Tune

In the normal position of this switch the HF Tuning Indicator indicates synchronism of the high frequency loop. When depressed, the HF Tuning Indicator indicates the amplitude of output of the 2 to 4 mc amplifier.

3. MCS

This selector tunes the synthesizer to the P.M.O. output frequency. The tuning is accomplished by first depressing the Push to Tune switch and adjusting the MCS selector for a maximum indication of the HF Tuning Indicator. Then releasing the Push to Tune switch, the MCS selector is readjusted for maximum amplitude of audio tone in the phones.

4. KCS

This selector selects the desired 1 kc digit.

5. CPS

These selectors select the desired hundreds digit. The lower cps selector synchronizes the low frequency loop as indicated by the L.F. Tuning Indicator.

II. PROCEDURE FOR ESTABLISHING A DESIRED OUTPUT FREQUENCY

1. Set the P.M.O. frequency dial to approximately the desired frequency.

2. Set the KCS and CPS selectors to the desired frequency.

3. Slowly vary the lower CPS selector in the neighborhood of the previously selected position until there is a deflection of the L.F. Tuning Indicator. Synchronism is accomplished when the movement of the lower CPS Selector causes a corresponding deflection of the L.F. Tuning Indicator. Readjust slightly until the L.F. Tuning Indicator reads center scale.

4. Depress the Push to Tune switch and tune the MCS selector for a maximum reading on the HF Tuning Indicator. Release the Push to Tune switch.

5. Retune the MCS selector for a maximum audio tone in the phones.

6. Adjust the P.M.O. Tuning for a zero-beat-note in the phones. The high frequency loop will then be synchronized. Movement of the P.M.O. tuning knob will cause a corresponding movement of the HF Tuning Indicator. Center the HF Tuning Indicator with the P.M.O. tuning knob.



ALIGNMENT PROCEDURE

I. Test Equipment

1. VTVM Hewlett-Packard 410B or equivalent.
2. Oscilloscope Tektronix 535 or equivalent.
3. Counter Hewlett-Packard 523 or equivalent.
4. Signal Generator: Measurements Signal Generator, Model 65B Standard, or equivalent.

II. Divider Chain

Align the divider chain as indicated in the general checkout procedure.

III. Low Frequency Loop

1. 1-2 kc Locked Oscillator

- a. Connect a counter to the 1-2 kc test point and a VTVM to the DC-1 test point. Since the DC voltage developed at DC-1 it can be either positive or negative with respect to ground. It is convenient to zero-center the VTVM on the 1 volt DC scale.
- b. Remove the 100 cps input signal to the low frequency deck and adjust the 1-2 kc Bal for zero DC volts at DC-1. Replace the 100 cps coaxial cable.
- c. Set the upper CPS selector to 900 and adjust C-9 until the loop is synchronized, i.e., when the VTVM indicates a DC voltage at DC-1 and the counter registers 1900 cps. While maintaining synchronism, adjust C-9 for zero volts at DC-1.
- d. Set the upper CPS selector to 800 and adjust the C-8 trimmer until the loop is synchronized. While maintaining the 1800 cps synchronized frequency adjust the trimmer for zero volts at DC-1.
- e. Repeat this procedure for the remaining positions of the upper CPS selector. Progress down in frequency one step at a time and make the adjustment for each step with the trimmer whose number corresponds to the upper CPS selector position. The correct frequency at the 1-2 kc test point for each CPS selector position is given in the general checkout procedure. When the loop is aligned, remove the counter and VTVM.

2. 9-18 kc Locked Oscillator

- a. Connect an oscilloscope to the PG-Out test point and adjust the Bias Adj. until a pulse 20 usec in width and occurring at a stable 1 kc rate is obtained. Correct adjustment will allow a stable pulse to be generated only when the 1 kc signal is applied to the low frequency deck. Remove oscilloscope.

b. Connect a zero-centered-VTVM to the DC-2 test point. Remove the 1 kc input signal to the low frequency deck and adjust the 9-18 kc Bal. for zero volts DC. Replace the 1 kc input coaxial cable.

c. Connect the counter to the 9-18 kc test point. Set the KC selector to the 9 position and adjust L-9 until the loop is synchronized, i.e., a D.C. voltage is indicated on the VTVM and the counter registers 18,000 cps. While maintaining the 18,000 cps synchronized frequency, adjust the L-9 for zero volts at DC-2. If the coil does not have sufficient range, the 9-18 kc padder may be adjusted to reposition the tuning range of the coil. Do not readjust the padder hereafter.

d. Set the KC selector to the 8 position and adjust L-8 until the loop is synchronized. While maintaining the 18,000 cps synchronized frequency, adjust L-8 for zero volts at DC -2.

e. Repeat the procedure for the remaining positions of the KCS selector. Progress down in frequency one step at a time and make the adjustment for each step with the coil whose number corresponds to the KCS selector position. The correct frequency at the 9-18 kc test point for each KCS position is given in the general checkout procedure. When the loop is aligned remove the counter and VTVM.

3. 510 to 520 kc Oscillator

a. Connect the counter to the 510 to 520 kc output jack.

b. Set the upper CPS selector to 900 and the Lower CPS selector to 500. This will assure that the main low frequency loop is not synchronized. Adjust the L.F. Bal. until the L.F. Tuning Indicator reads center scale.

c. Set the KCS selector to 9 and set both of the CPS selectors to 500. Adjust the P-9 until the main low frequency loop is synchronized, i.e., adjustment of P-9 will position the L.F. Tuning Indicator and the counter will register 519,500 cps. Adjust P-9 until the L.F. Tuning Indicator reads center scale.

d. Set the KCS selector to 8 and adjust P-8 until the main control loop is synchronized. While maintaining the 518,500 cps synchronized frequency, adjust P-8 for a center scale reading of the L.F. Tuning Indicator.

e. Repeat this procedure for the remaining positions of the KCS selector. Progress down in frequency one step at a time and make the adjustment for each step with the trimmer whose number corresponds to the KCS selector with the CPS selector at 500 and the loop synchronized.



<u>KCS Position</u>	<u>Output Frequency</u>
9	519,500
8	518,500
7	517,500
6	516,500
4	514,500
5	515,500
3	513,500
2	512,500
1	511,500
0	510,500

When the loop is aligned, remove the counter.

IV. High Frequency Loop

1. Harmonic Selector

- a. Remove the 510 to 520 kc input from the low frequency deck, the 2 to 4 MC input from the P.M.O., and the 6AX5 pulse generator tube.
- b. Connect the signal generator to the Pulse Out test point and the oscilloscope to the Har Sel Out test point.   
*IN GRID V205*
- c. Set the MCS selector to 2 MC position (full mesh) and the signal generator to 1.49 MC at 2 volts. Adjust L<sub>1</sub> and L<sub>2</sub> for maximum amplitude   
*V206 PLATE*
- d. Reset the MCS selector to the 4 MC position (full open) and the signal generator to 3.49 MC at 2 volts. Adjust the trimmers on both ends of the 3 ganged tuning capacitor for maximum amplitude.
- e. Repeat steps c. and d. until the selected signal is a maximum at both positions without further adjustments.
- f. Reconnect the 2 to 4 MC input from the P.M.O.

2. 2- to 4 MC Isolation Amplifier and Harmonic Selector Tracking

- a. Set the signal generator at 2.37 MC at 2 volts and the P.M.O. dial to 2.88 MC   
*510kc*
- b. Adjust MCS selector for maximum amplitude on scope.
- c. Connect oscilloscope to I.A. Out. Adjust L-3 for maximum amplitude.   
*PLATE V-201*
- d. Set both the MCS selector and P.M.O. frequency to 2.00 MC. Adjust C-4 for maximum amplitude.

e. Set both the MCS selector and P.M.O. frequency to 4 MC. Adjust the trimmer capacitor, on the center section of the 3 ganged tuning capacitor, for maximum amplitude.

f. Repeat steps a. through e as many times as is necessary to make the tracking exact at these points.

g. Remove the 2 to 4 MC input, oscilloscope and the signal generator.

### 3. IF Strip

a. Connect the signal generator to the I.A. Out test point. Set the signal generator to 515 kc at 2 volts. Connect the oscilloscope to the I.F. Out test point.

b. Adjust  $L_4$ ,  $L_5$ , and  $L_6$  for maximum amplitude.

c. Remove the signal generator and the oscilloscope. Connect the 2 to 4 MC and 510 to 520 kc inputs to the deck. Replace the 6AK5.

### 4. 0.2 usec Pulse Generator

a. Connect the oscilloscope to the PG-Out test point and adjust the Bias Adj. until a pulse 0.2 usec in width and recurring at a stable 10 kc rate is obtained.

b. Remove the 10 kc input and verify that there is no output at the PG-Out test point, to insure proper bias adjustment.

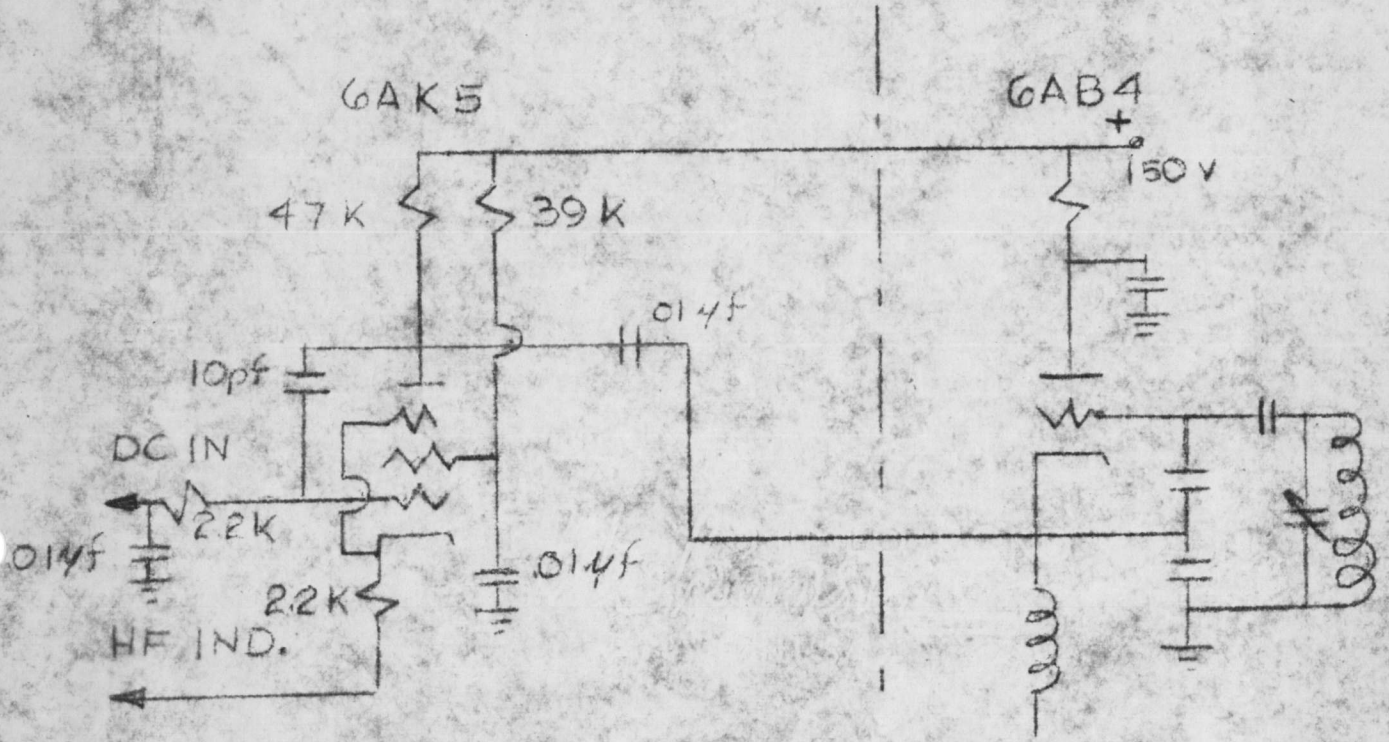
### 5. H.F. Phase Detector

a. Set the MCS selector to a frequency differing at least 100 kc from the P.M.O. frequency. This will insure that the high frequency loop is not synchronized.

b. Adjust the H.F. Bal. for center scale on the H.F. Tuning Indicator.



# MODIFICATION OF PMO

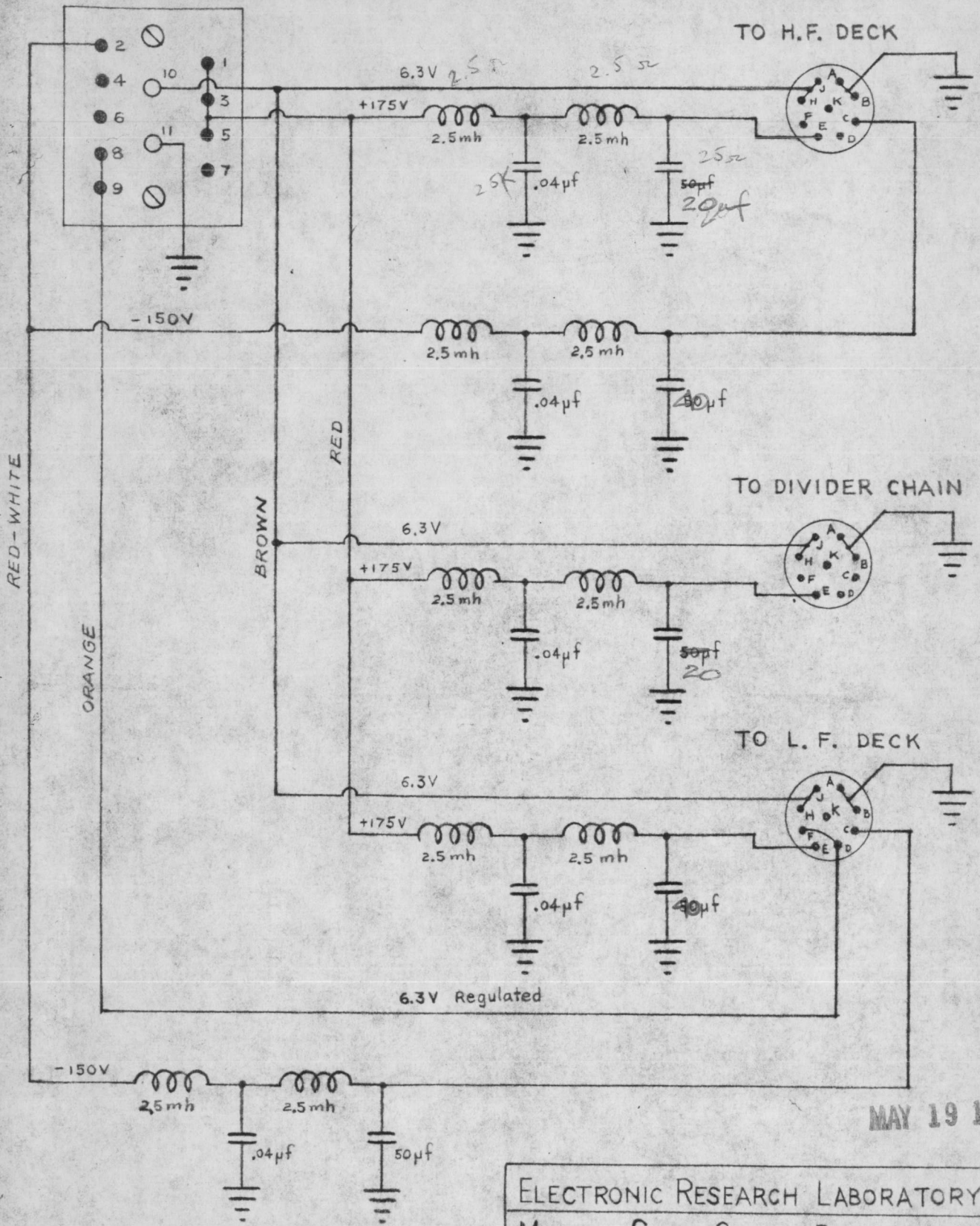


Note: Added 6AK5  
 Replaced V301 (6C4) with 6AB4 requiring  
 pins 1 & 5 to be connected together.

MSC FRL  
 11-11-68  
 CPE





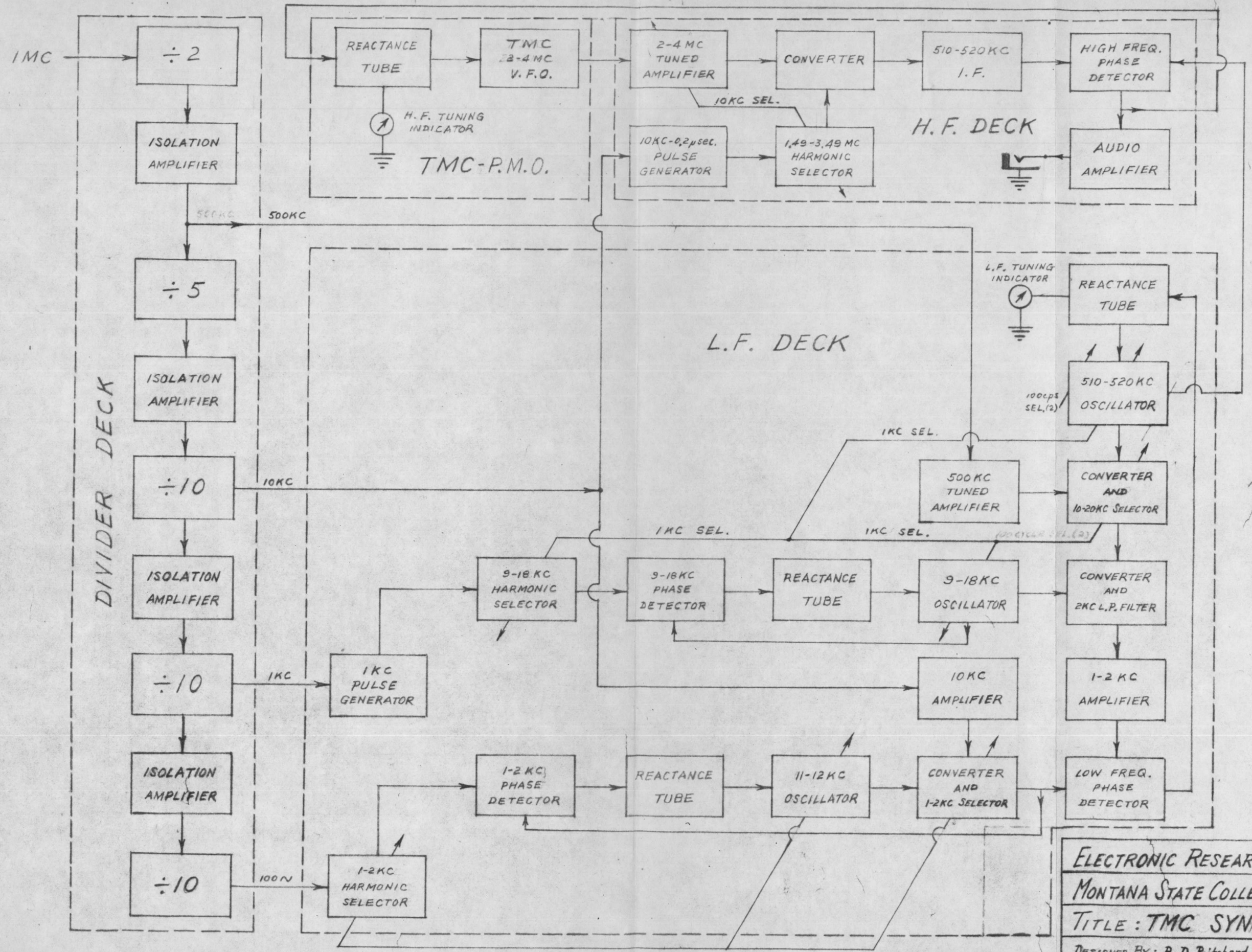


MAY 19 1958

ELECTRONIC RESEARCH LABORATORY	
MONTANA STATE COLLEGE, BOZEMAN, MONT.	
TITLE: LINE FILTER	
DESIGNED BY: W.E. Beadle.	DATE: 9-5-1958
DRAWN BY: George Cheng.	DATE: 9-5-1958

TMC # CK-388





MAY 19 1959

ELECTRONIC RESEARCH LABORATORY  
 MONTANA STATE COLLEGE, BOZEMAN, MONT.  
 TITLE: TMC SYNTHESIZER  
 DESIGNED BY: B. D. Pritchard & W. E. Beadle  
 ADVISER: D. K. Weaver, Jr.

TMC # CK-387

100 CYCLE SEL. (1)







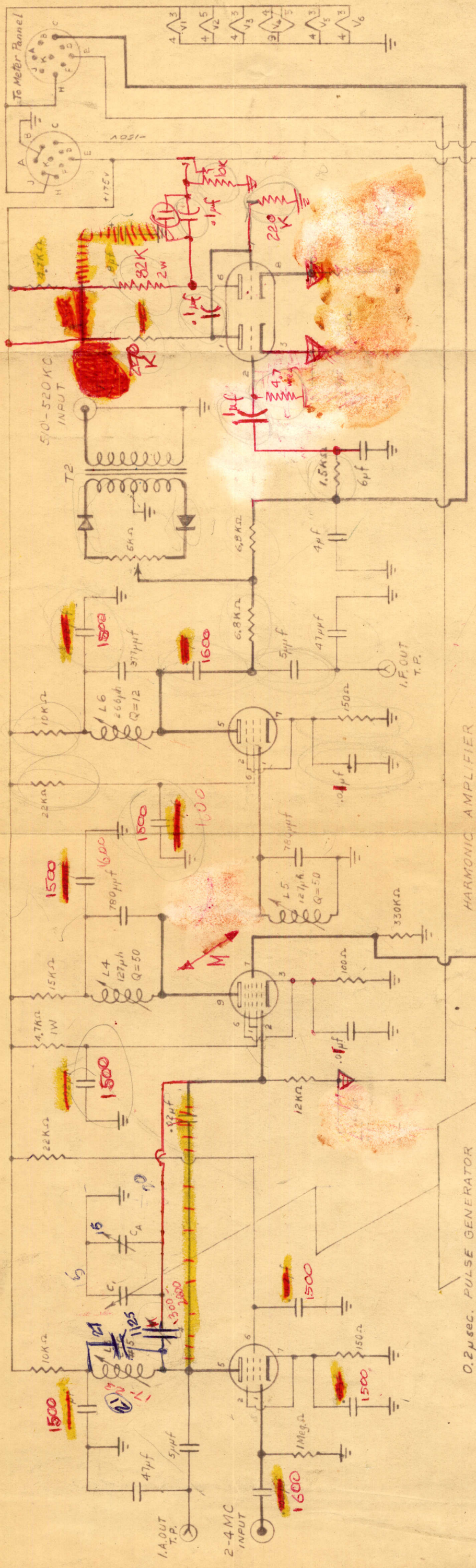
2-4 MC ISOLATION AMPLIFIER  
6AU6 V1

CONVERTOR  
6BA7 V2

IF AMPLIFIER  
6AU6 V3

PHASE DETECTOR  
12AT7 V4

AUDIO AMP  
12AT7 V4



0.2 μsec. PULSE GENERATOR  
6AK5 V5

HARMONIC AMPLIFIER  
6AU6 V6

ALL RESISTORS: 1/2 WATT UNLESS OTHERWISE SPECIFIED.  
ALL DIODES: 1N100.  
C1, C2, & C3: 10-365 μf - 3 GANGED AIR VARIABLE CAPACITORS.  
C4, C5, & C6 ARE ASSOCIATED TRIMMERS.  
C4: 1300-2830 μf MICA PADDER.  
T1: STAT-TRAN (Pulse Engineering) EF 71 - 0.2 μsec. PULSE TRANSFORMER. TURNS RATIO 1:1.  
T2: PRIMARY-5 TURNS #21; SECONDARY - 50 TURNS, #26.  
BIFILAR WOUND, 50 Ω to 5000 Ω.  
CORE MATERIAL: FERROX CUBE POT CORE.  
FXC. 3B3 PART NO. 273P236E1 - 3B3.

MAY 19 1963

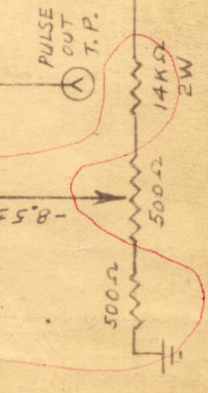
ELECTRONIC RESEARCH LABORATORY  
MONTANA STATE COLLEGE, BOZEMAN, MONT.  
TITLE: HIGH FREQUENCY LOOP

DESIGNED BY: W. E. Beadle  
DRAWN BY: Gerry  
DATE: 10/10/1951

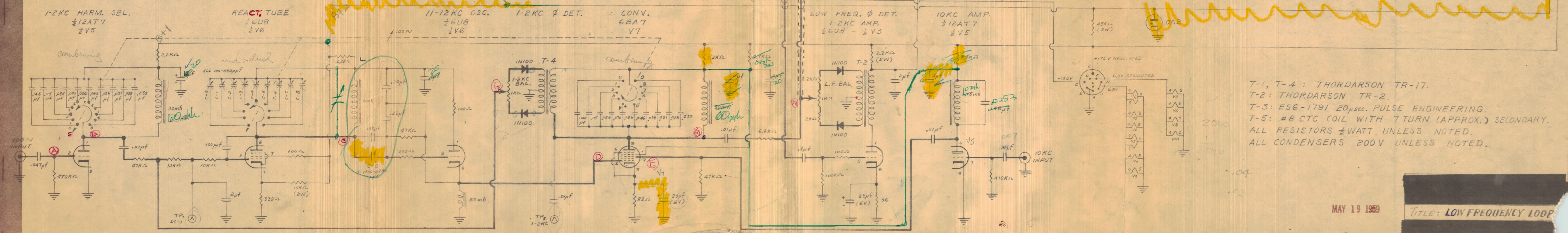
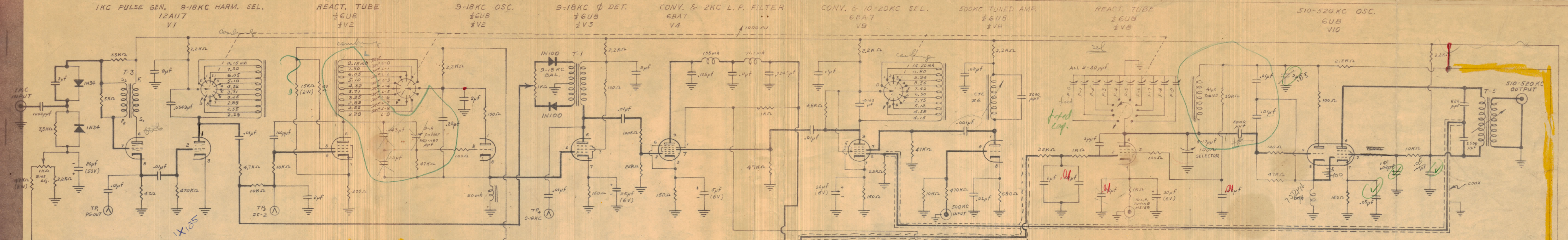
TMC # CK-385

225  
170  
195  
17  
400  
340

Bias Adj.







T-1, T-4: THORDARSON TR-17.  
 T-2: THORDARSON TR-2.  
 T-3: ES6-1791 20 $\mu$ sec. PULSE ENGINEERING.  
 T-5: #8 CTC COIL WITH 7 TURN (APPROX.) SECONDARY.  
 ALL RESISTORS  $\frac{1}{2}$  WATT, UNLESS NOTED.  
 ALL CONDENSERS 200V UNLESS NOTED.

MAY 19 1959

TITLE: LOW FREQUENCY LOOP

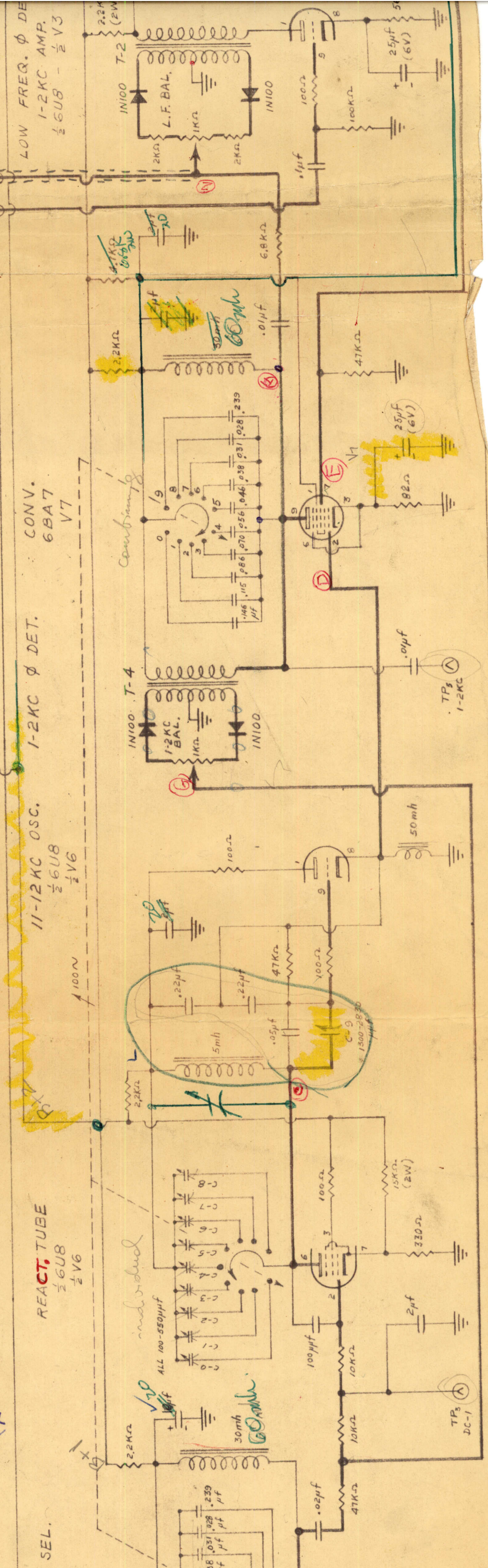
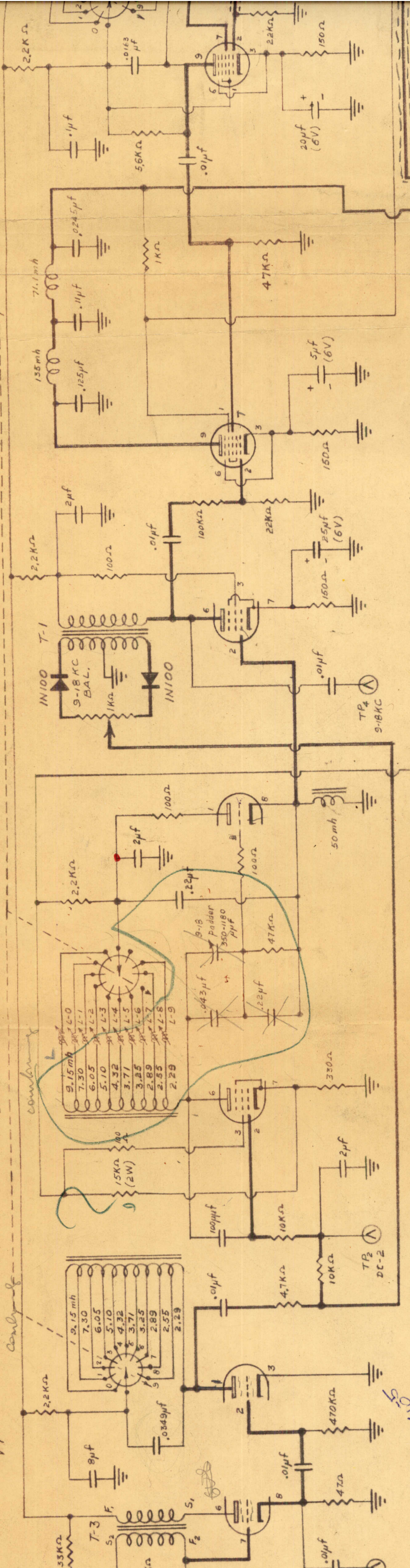
TMC # CK-384







CONV. & 10-20  
 6BA7 V9  
 CONV. & L.P. FILTER  
 6BA7 V4  
 9-18KC  $\phi$  DET.  
 6U8  $\frac{1}{2}$  V3  
 9-18KC OSC.  
 6U8  $\frac{1}{2}$  V2  
 REACT. TUBE  
 6U8  $\frac{1}{2}$  V1  
 PULSE GEN. 9-18KC HARM. SEL.  
 12AU7 V1  
 CONV. & 10-20  
 6BA7 V9  
 CONV. & L.P. FILTER  
 6BA7 V4  
 9-18KC  $\phi$  DET.  
 6U8  $\frac{1}{2}$  V3  
 9-18KC OSC.  
 6U8  $\frac{1}{2}$  V2  
 REACT. TUBE  
 6U8  $\frac{1}{2}$  V1  
 PULSE GEN. 9-18KC HARM. SEL.  
 12AU7 V1

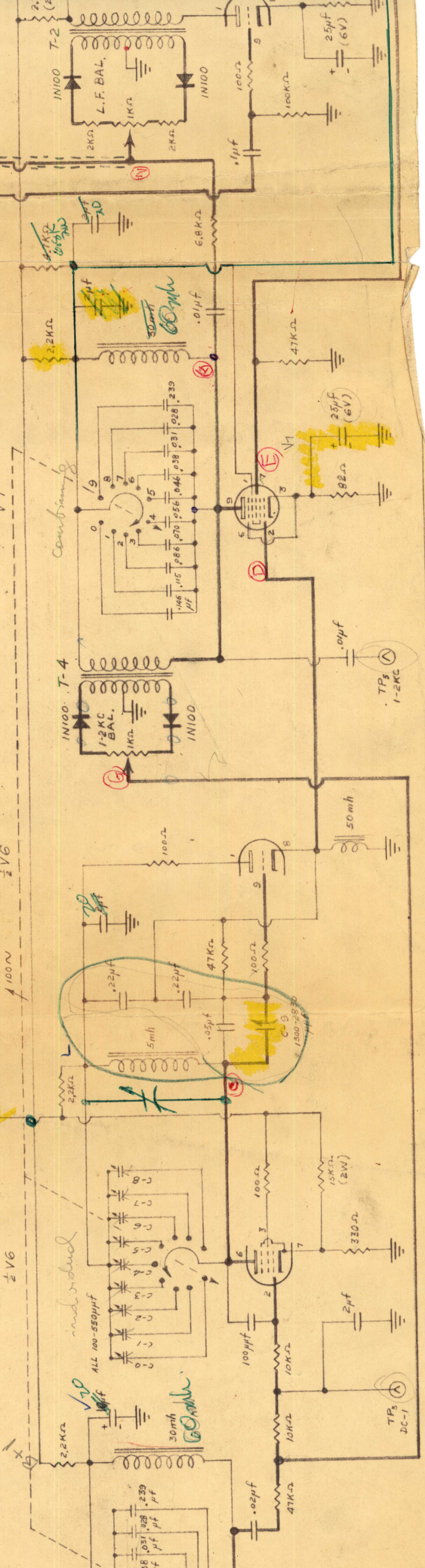


LOW FREQ.  $\phi$  DE  
1-2KC AMP.  
6U8 - 1/2 V3

CONV.  
6BA7  
V7

REACT. TUBE  
6U8  
1/2 V6

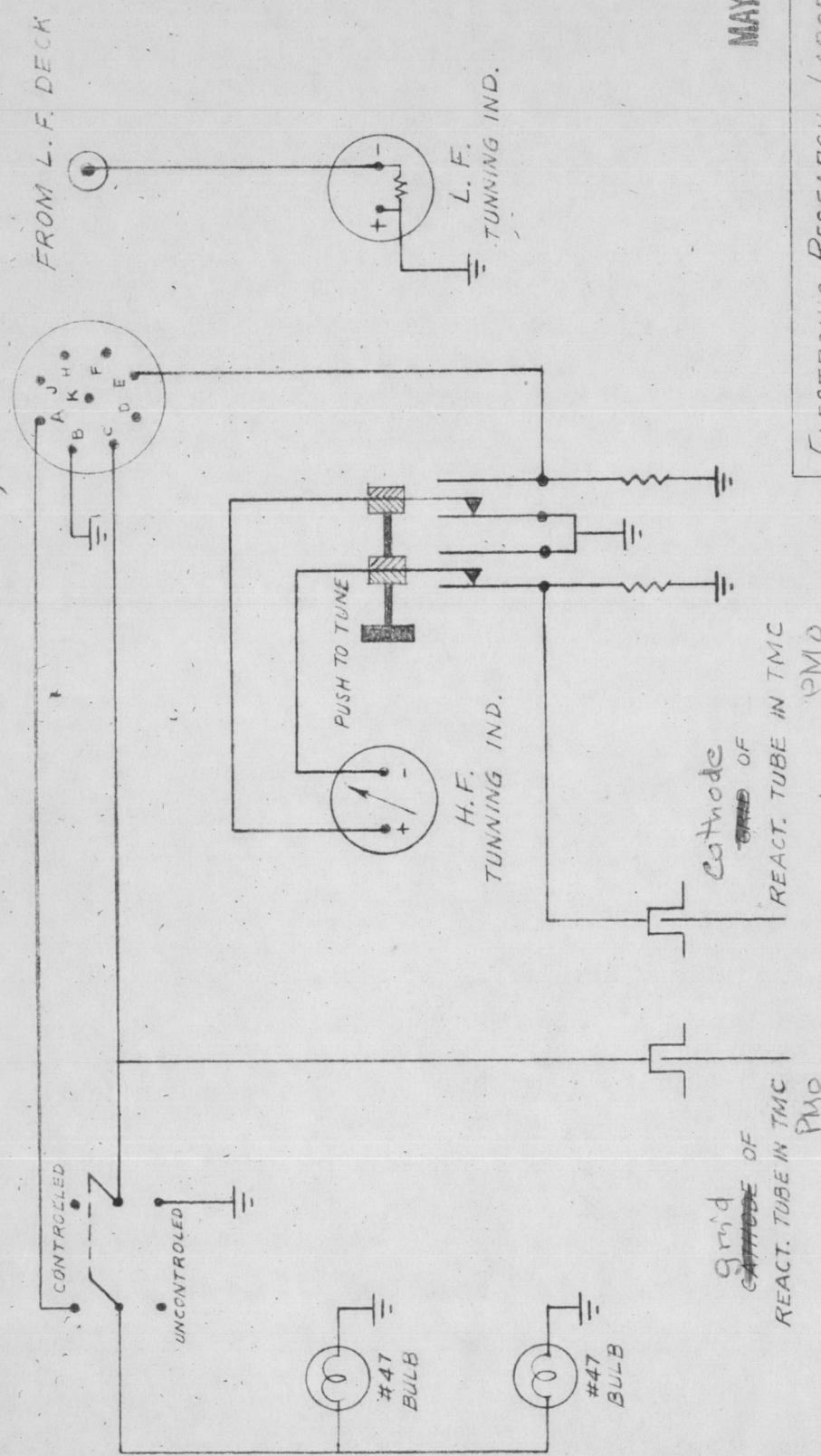
SEL.











MAY 19 1958

ELECTRONIC RESEARCH LABORATORY	
MONTANA STATE COLLEGE, BOZEMAN, MONT.	
TITLE: METER PANNEL	
DESIGNED BY: W.E. Beadle	DATE: 9-23-1958
DRAWN BY: GEORGE CHENG	DATE: 9-24-1958

TMC # CK-389

Grid  
CATHODE OF  
REACT. TUBE IN TMC  
PMD

Cathode  
OF  
REACT. TUBE IN TMC  
PMD