TECHNICAL MANUAL

for

SIGNAL DATA CONVERTER-STORER MODEL RTMU-41A

THE TECHNICAL MATERIEL CORPORATION

MAMARONECK, N.Y. OTTAWA, CANADA

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MAMARONECK, N.Y. OTTAWA, CANADA

005702052 ISSUE DATE: MAY 1970

NOTICE

RECORD OF CORRECTIONS MADE

Change No.	Date of Change	Date Entered	Entered By

THE TECHNICAL MATERIEL CORPORATION
COMMUNICATIONS ENGINEERS
700 FENIMORE ROAD MAMARONECK. N. Y.

Warranty

The Technical Materiel Corporation, hereinafter referred to as TMC, warrants the equipment (except electron tubes,* fuses, lamps, batteries and articles made of glass or other fragile or other expendable materials) purchased hereunder to be free from defect in materials and workmanship under normal use and service, when used for the purposes for which the same is designed, for a period of one year from the date of delivery F.O.B. factory. TMC further warrants that the equipment will perform in a manner equal to or better than published technical specifications as amended by any additions or corrections thereto accompanying the formal equipment offer.

TMC will replace or repair any such defective items, F.O.B. factory, which may fail within the stated warranty period, PROVIDED:

1. That any claim of defect under this warranty is made within sixty (60) days after discovery thereof and that inspection by TMC, if required, indicates the validity of such claim to TMC's satisfaction.
2. That the defect is not the result of damage incurred in shipment from or to the factory.
3. That the equipment has not been altered in any way either as to design or use whether by replacement parts not supplied or approved by TMC, or otherwise.
4. That any equipment or accessories furnished but not manufactured by TMC, or not of TMC design shall be subject only to such adjustments as TMC may obtain from the supplier thereof.

Electron tubes*furnished by TMC, but manufactured by others, bear only the warranty given by such other manufacturers. Electron tube warranty claims should be made directly to the manufacturer of such tubes.

TMC's obligation under this warranty is limited to the repair or replacement of defective parts with the exceptions noted above.

At TMC's option any defective part or equipment which fails within the warranty period shall be returned to TMC's factory for inspection, properly packed with shipping charges prepaid. No parts or equipment shall be returned to TMC, unless a return authorization is issued by TMC.

No warranties, express or implied, other than those specifically set forth herein shall be applicable to any equipment manufactured or furnished by TMC and the foregoing warranty shall constitute the Buyers sole right and remedy. In no event does TMC assume any liability for consequential damages, or for loss, damage or expense directly or indirectly arising from the use of TMC Products, or any inability to use them either separately or in combination with other equipment or materials or from any other cause.

*Electron tubes also include semi-conductor devices.

PROCEDURE FOR RETURN OF MATERIAL OR EQUIPMENT

Should it be necessary to return equipment or material for repair or replacement, whether within warranty or otherwise, a return authorization must be obtained from TMC prior to shipment. The request for return authorization should include the following information:

1. Model Number of Equipment.
2. Serial Number of Equipment.
3. TMC Part Number.
4. Nature of defect or cause of failure.
5. The contract or purchase order under which equipment was delivered.

PROCEDURE FOR ORDERING REPLACEMENT PARTS

When ordering replacement parts, the following information must be included in the order as applicable:

1. Quantity Required.
2. TMC Part Number.
3. Equipment in which used by TMC or Military Model Number.
4. Brief Description of the Item.
5. The *Crystal Frequency* if the order includes crystals.

PROCEDURE IN THE EVENT OF DAMAGE INCURRED IN SHIPMENT

TMC's Warranty specifically excludes damage incurred in shipment to or from the factory. In the event equipment is received in damaged condition, the carrier should be notified immediately. Claims for such damage should be filed with the carrier involved and not with TMC.

All correspondence pertaining to Warranty Claims, return, repair, or replacement and all material or equipment returned for repair or replacement, within Warranty or otherwise, should be addressed as follows:

THE TECHNICAL MATERIEL CORPORATION
Engineering Services Department
700 Fenimore Road
Mamaroneck, New York

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GENERAL INFORMATION

1-1. GENERAL DESCRIPTION

a. Functional Description - The Signal Data Converter-Storer is a combination of serial-to-parallel converter and temporary storage (memory) device for information transmitted in teletype code. It is used at a remote-controlled equipment site to receive teletype tuning codes from the remote control site. In this operation, it works in conjunction with a decoder unit, the function of which is to receive the codes from the RTMU and position the transmitter or receiver system (hereinafter referred to as equipment) controls accordingly.

The converter section of the RTMU receives teletype codes in serial pulse form from standard teletype receiving equipment and converts the bits of the codes into a parallel form for introduction into the memory section.

The memory section receives and stores the code bits (representing tuning commands for the equipment). Upon receiving the end code (a teletype "E") a triggering signal is sent to the associated decoder, setting up a reciprocating action between the RTMU and the associated decoder. In this process, codes are drawn out of the RTMU and processed by the decoder to move the equipment controls.

The RTMU-41A can process a 5-bit code contained in any manually keyed teletype transmission from a 5-level up to an 8-level system by taking information out of the first five bits in the code. In a transmis n from punched tape, the RTMU-41A can process a 5-level pattern only. The unit contains an isolation keyer at its input, designed to work directly from a teletype current loop. A recognition code in the beginning of the tuning message opens a particular RTMU unit for the rest of the message and this is determined by a matrix wiring on a parallel shift-register plug-in card. Up to fifty codes are available for this purpose. An array of equipments can, in this way, be tuned from the same teletype current loop. The RTMU-41A can consecutively feed five equipments (each with a different tuning message). Each recognition code consists of a letter, A through E, and a number, 1 through 5, representing the block and the equipment, respectively. (See table 1-3.)

In the RTMU-41A the recognition code, besides selecting a particular equipment, also triggers a readback of control positions from the selected equipment. The readback to the remote operator, originating from the associated decoder, is used as a check against the tuning message sent.

b. Physical Description - The RTMU-41A (see figure 1-1) is constructed to serve as a 19-inch rack-mounted unit. All circuitry is solid state, employing negative binary logic components, and mounted on plug-in printed circuit cards and assemblies. Standardized integrated circuits are used wherever applicable. The front panel is 19 inches wide x 5-1/4 inches high x 3/16 inches thick and is finished in light gray enamel per MIL-E-15090. The chassis is 17 inches wide and extends 17 inches behind the panel. The complete RTMU-41A unit weighs approximately 30 pounds.

1-2. DESCRIPTION OF PLUG-IN CARDS

Table 1-1 is a list of printed circuit plug-in cards used in the RTMU-41A. Power circuitry design includes a short-proofing feature to prevent damage to a card that is plugged into the wrong socket.

1-3. REFERENCE DATA

Table 1-2 lists quick-reference technical data on the Signal Data Converter-Storer. This table includes nominal specification figures defining the unit.

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Figure 1-1. Signal Data Converter-Storer

TABLE 1-1. PLUG-IN CARD COMPLEMENT

Card Circuit Symbols	Function	TMC Part No.
A1	Isolation Keyer Card	A4494
A2	Clock Timing Circuit Card	A4565
A3	Parallel Shift Register Card	A4566
A4	Gating Circuit Card	A4567
A6	Shift Timing Circuit Card	A4569
A7	Integrated Shift Register Card	A4710
A10	Power Supply Card	A4549
A11	Readback Selector Assy	AX5009

TABLE 1-2. TECHNICAL SPECIFICATIONS

Code input:	5-bit codes in teletype transmission in 20 ma or 60 ma neutral or polar, teletype loop, across 25,000 ohms. Serial pulses in 5-level with 8-level* pattern at 45 baud. 1 = current; 0 = no current.
Code output:	5-level parallel voltage pulses. 1 -8V to -10VDC; 0 = 0 to -0.5VDC
Recognition Code:	As specified on order. See table 1-3 for selection.
Specific Codes:	"Tune" code (10000). "Clear" code (01111).
Power Requirements:	115/230 VAC, 50/60 cps, single phase.
Average power consumption:	60 watts
Ambient temperature and humidity:	0 to 50°C and up to 95% relative humidity
Overall dimensions:	5-1/4 inches high x 19 inches wide x 17 inches deep.
Weight:	Approximately 30 pounds.

*In 8-level pattern, uses first 5 bits.

TABLE 1-3. AVAILABLE RECOGNITION CODES

Select Function		Code Bits	Teletype Characters		Jumper X-To-Y Wiring On PAR. Shift Rgstr Card A3 (P/N A4566)				
		12345	CCIT	ASCH*	X1	X2	X3	X4	X5
EQUIPMENT BLOCK	A	10101	Y	U	Y1	Y4	Y5	Y8	Y9
	B	10110	F	M	Y1	Y4	Y5	Y7	Y10
	C	11010	J	K	Y1	Y3	Y6	Y7	Y10
	D	11001	W	S	Y1	Y3	Y6	Y8	Y9
	E	10011	B	Y	Y1	Y4	Y6	Y7	Y9
EQUIPMENT	1	00010	Carriage Return	H	Y2	Y4	Y6	Y7	Y10
	2	01010	R	J	Y2	Y3	Y6	Y7	Y10
	3	01100	I	F	Y2	Y3	Y5	Y8	Y10
	4	01000	Line Feed	B	Y2	Y3	Y6	Y8	Y10
	5	00100	Space	D	Y2	Y4	Y5	Y8	Y10

*Only the first five bits of the 7-bit code are utilized.

SECTION II
INSTALLATION

2-1. UNPACKING AND HANDLING

Inspect the RTMU packing case for possible damage when it arrives at the operating site. With respect to damage of the equipment for which the carrier is liable, the Technical Material Corporation will assist in describing methods of repair and the furnishing of replacement parts.

2-2. POWER REQUIREMENTS

The RTMU leaves the factory wired to operate from a 115-VAC 50/60-cps, single-phase source. The Converter-Storer can be rewired for a 230-VAC, 50/60-cps, single-phase source by jumping connections to place the two sections of transformer T1 primary coil (see figure 2-1) in series with one another across the 230 volts. When performing this change, maintain the 115-VAC connections across the blower as shown in figure 2-1 using one half of the primary coil.

2-3. INSTALLATION REQUIREMENTS

a. General - When the RTMU unit arrives as part of a specific transmitter or receiver system (such as the DDRR-10K or DDRR-10M Receiving Sets or GPTR-10KYA Transmitter System), specific instructions for installing this module are included in Section 2 of the specific Equipment System manual. The following text, therefore, is to be used only if the RTMU has been obtained as a separate item for making up an equipment system not contracted for.

Capabilities of the RTMU depend on associated equipment in the system.

b. Mechanical Installation - Outline dimensions for the RTMU-41A are listed in table 1-2. The unit may be mounted by its front panel with or without accompanying drawer slides. Drawer slides for the RTMU are tilt-lock type and will be shipped with the unit when specified on order.

To install drawer slides; install external parts (rack sections) into rack, and install internal parts onto RTMU chassis sides, using existing threaded inserts in the chassis. Then proceed as follows, referring to figure 2-2:

(1) Pull center sections of rack-mounted slide sections out until they lock in an extended position.

(2) Position internal part (RTMU mounted) of slide in tracks of the external section and ease RTMU into rack until release buttons engage holes in track.

(3) Make cable connections as required at rear panel of RTMU (see table 2-1). Include ground jumper connection to rack structure.

(4) Depress release buttons and slide component completely into rack.

c. Electrical Installation - Table 2-1 lists all of the electrical connectors on the RTMU and their functions. Figure 2-3 shows connector locations. Included in table 2-1 are part numbers for connectors and for their mating plugs, (included in shipment when the RTMU is ordered alone). Refer to figure 2-4 for wiring details of RTMU. Connect jumpers per station requirements in accordance with the "Equipment Selection Jumper Guide" on figure 7-4.

2-4. CABLE ASSEMBLIES

To fabricate specific cable assemblies, refer to table 2-1 for mating plugs and figure 2-4 for specific wiring details.

2-5. INSPECTION AND ADJUSTMENT

a. Test Equipment - The test equipment required for inspection and adjustment of the RTMU-41A are listed in table 2-2.

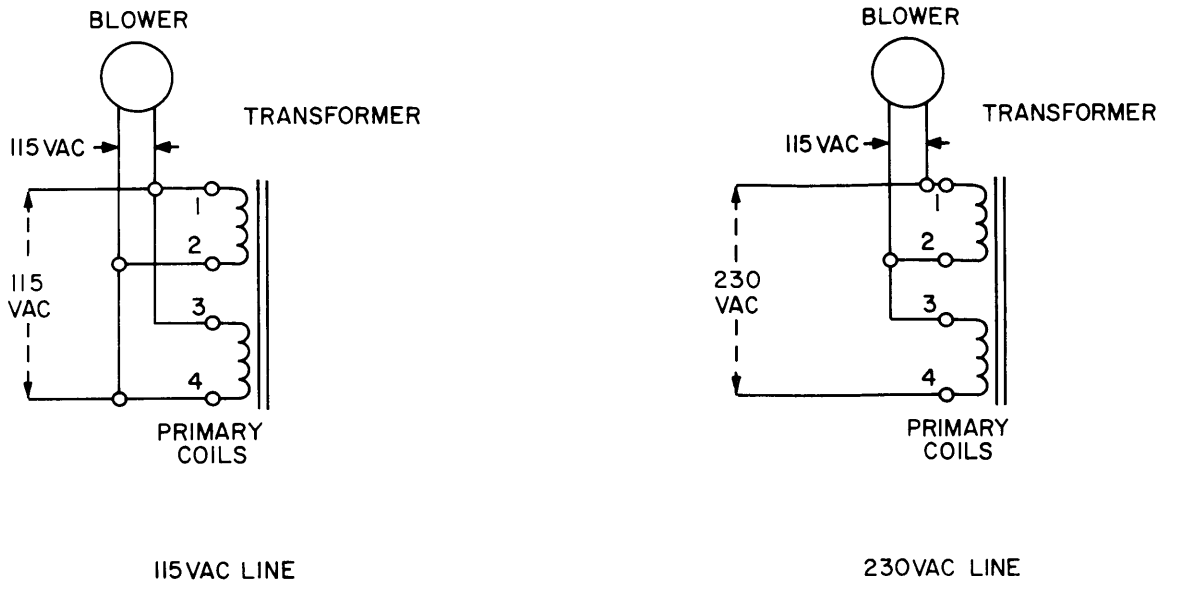

Figure 2-1. 230 VAC 115 VAC Transformer Wiring

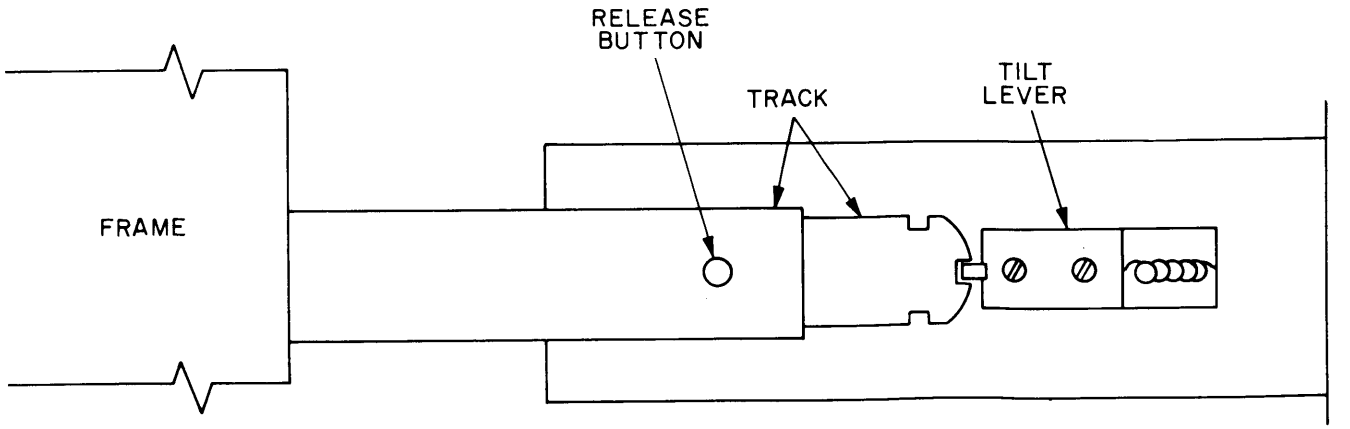

Figure 2-2. Slide Mount Details

TABLE 2-1. ELECTRICAL CONNECTORS

Receptacle Ref Designation	Function	Receptacle Type and Part No.	Mating Plug Type and Part No.
J1	115/230 VAC line voltage input	MS3102-16S-5P	MS3106-16S-5S
(A11) J2	Readback TTY code output, equipment #1; inputs from decoders #1-5	50-pin, male, fixed screwlock receptacle shell and mounting plate, #JJ333-50PFS34.	50-pin, female, rotating screwlock, plug shell and hood, #JJ333-50SRS12.
J3	Code output to decoder. Signal exchange between RTMU and decoder.	50-pin, female, fixed screwlock, receptacle shell and mounting plate, #JJ333-50SFS34.	50-pin, male, rotating screwlock, plug shell and hood, #JJ333-50PRS12.
J4	Teletype tuning code input	9-pin, male, fixed screwlock, receptacle shell and mounting plate, #JJ333-9PRS34.	9-pin, female, rotating screwlock, plug shell and hood, #JJ333-9SRS12.

TABLE 2-2. TEST EQUIPMENT REQUIRED

Equipment	Manufacturer and Part No.
VOM	Simpson Model 260, or equivalent
Frequency Counter	Hewlett-Packard 5244L, or equivalent
Oscilloscope	Tektronix Model 541A, or equivalent
Teletypewriter	45.45 Baud, 7.42 unit code
D.C. Loop Supply	Station Battery

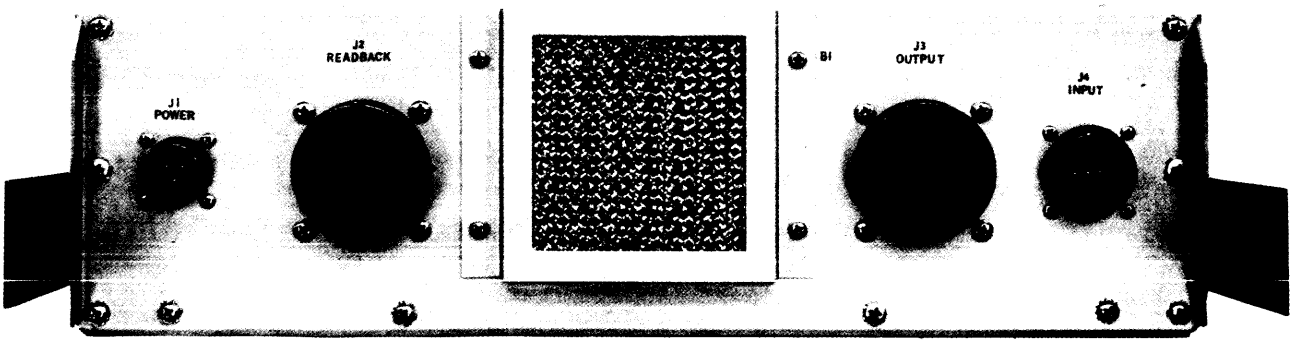

Figure 2-3. Rear Panel Connector Locations

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b. Initial Checkout - To perform an initial checkout of the RTMU-41A, proceed as follows:

(1) Preliminary Electrical Test

a. Ensure that plug is removed from power connector J1.

CAUTION

Plug must be removed from power connector J1. Failure to do so will result in serious damage to VOM.

b. Connect VOM across pins A and C of J1. Meter should indicate no continuity.

c. Set primary power ON/OFF switch S1 to ON. Meter should indicate continuity (approximately 4 ohms).

d. Continuity should not exist between AC leads and ground.

e. Set primary power ON/OFF switch S1 to OFF and remove VOM.

f. Replace plug to J1.

c. Power Supply Voltage Checks

(1) Set POWER switch to "ON". POWER indicator will light. Removing either fuse will cause the power light to go out.

(2) Check voltage levels at test points +12VDC and -12VDC. Voltages should be as indicated ±1VDC. Check voltage at test point -27VDC ± 2V.

(3) Monitor TP +12V and jumper TP +12V to ground. Remove ground. Voltage level should return to +12VDC ± 1V. Repeat this test for test points -12VDC and -27VDC.

(4) Monitor TP +12V with a high gain scope. Ripple present on TP +12V should be no more than 20 millivolts peak-to-peak. Repeat for test points -12VDC and -27VDC.

(5) Set POWER switch to "OFF". Connect scope probe to DC reset test point. Set POWER switch to "ON". Level on DC reset test point should rise to approximately +3VDC and then fall and remain at approximately -5VDC.

(6) Measure following points for voltages and grounds.

CONNECTOR	PIN		
	+12VDC	-12VDC	GROUND
A1	--	4	1, 22, A, Z
A2	20	4	1, 22, A, Z
A3	20	4	1, 22, A, Z
A4	20	4	1, 22, A, Z
A6	20	4	1, 22, A, Z
A7	20	4	1, 22, A, Z

d. Functional Checks

(1) Set POWER switch to "OFF".

(2) Remove card A1 and measure resistance between pins 12 and 15 on A1 card and confirm that the resistance is in accordance with the teletype loop application, i.e.: when using a 60 ma loop, a strap should be connected across resistor R6 and the resistance measured between pins 12 and 15 should be 100 ohms ±10%. When using a 20 ma loop, no strap should be across R6 and the resistance should be 320 ohms ±10%.

(3) Connect a teletypewriter machine and D.C. loop supply to J4 input per figure 2-4.

(4) Insert extender card between card A1 and its socket XA1. Set POWER switch "ON". On teletypewriter keyboard send a series of alternate 'Y's and 'R's. During receipt of the corresponding alternate '1's and '0's, observe signal between pins 4 and B on extender card and adjust potentiometer R4, if necessary, until the pulse durations for the '1's and '0's are equal. Set POWER switch "OFF". Remove extender card and insert card A1 into its socket, XA1.

(5) Insert extender card between card A2 and its socket XA2. Connect a jumper between pin 4 and TP4 on A2 card. Set POWER switch "ON". The jumper will cause the clock in card A2 to generate pulses. Connect frequency counter to TP15 and adjust potentiometer, R2, for 27.00 msec. or 44 msec. ±0.05 msec. Set POWER switch "OFF". Disconnect counter and jumper. Remove extender card and return card A2 to its socket, XA2.

(6) Initiate a program as per table 4-1 via teletypewriter and observe corresponding equipment response. Also observe the teletypewriter printer to ensure that readback information confirms initiated program.

DECODER NO.1

4 5 GND

k h f

NING
OUTPUT

NG
PUT

D

STUNT LINE

GND

Q K

P/O TMC
P/N JJ333
50PRSI2
PLUG

JUMP TO J4-E AND -F
AND J3-Q AND -K OF
RTMU-41A UNIT IN
NEXT BLOCK OF FIVE
EQUIPMENTS

4 3 W R P M E

MEMORY ADVANCE SIGNAL INPUT
DECODER INHIBIT SIGNAL OUTPUT
START TUNE SIGNAL OUTPUT NO.1
MEMORY INHIBIT SIGNAL INPUT
MEMORY POWER SIGNAL OUTPUT
EQUIP SEL SIGNAL OUTPUT
GND

JUMP CONNECTOR BETWEEN DECODER NO.1 THRU NO. 5

TO DECODER

NO. 2 NO. 3 NO. 4 NO. 5

V U T S

NO. 2 NO. 3 NO. 4 NO. 5

START TUNE SIGNAL OUTPUT

P/O TMC P/N JJ333-50SRSI2 PLUG

FROM JUMPED CONNECTIONS IN DECODERS NO.1 THRU NO.5

N M

P/O (AII) J2 READBACK

-30V INPUT

GND

J1
AC PWR

A C B

115/230 VAC,
1φ 50/60Hz INPUT

TMC P/N
CA581-2-12
POWER CABLE

READBACK OUTPUT FROM DECODER

NO.1 NO.2 NO.3 NO.4 NO.5

(0) (1)

COM MARK SPACE

NO.1 NO.2 NO.3 NO.4 NO.5

INPUTS TO READ-BACK SELECTOR

OUTPUT FROM RDBK SELECTOR

(0) (1)

REPRE-SENTATIVE CONNECTIONS

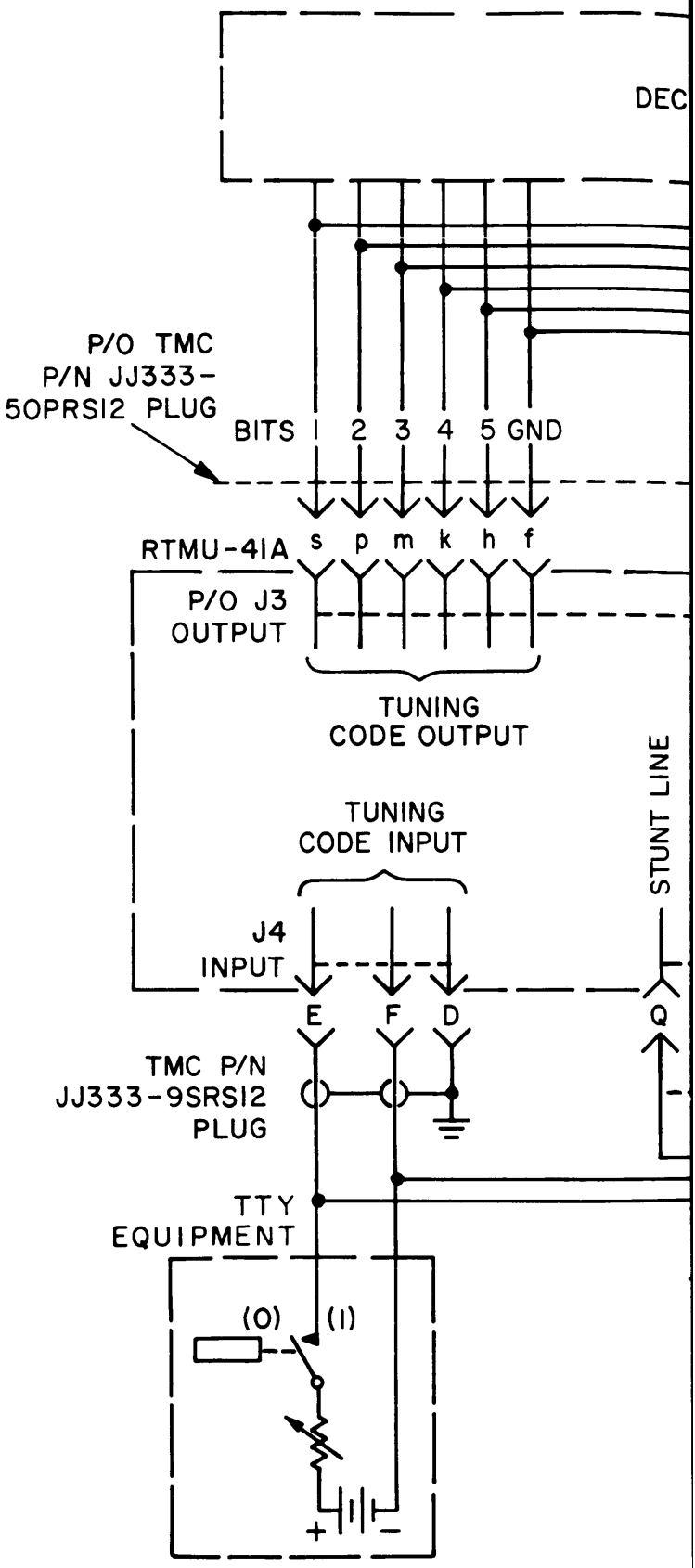
P/O (AII) J2

P/O TMC P/N
JJ333-50SRSI2
PLUG

TTY
EQUIPMENT

NOTE: THESE CONNECTIONS ARE BASED UPON ONE RTMU-41A CONTROLING ONE BLOCK OF FIVE EQUIPMENTS WITH ONE DECODER IN EACH EQUIPMENT

Figure 2-4. Wiring Connection Details


DEC
P/O TMC
P/N JJ333-
50PRSI2 PLUG
BITS 1 2 3 4 5 GND
RTMU-41A
s p m k h f
P/O J3
OUTPUT
TUNING
CODE OUTPUT
TUNING
CODE INPUT
J4
INPUT
E F D
Q
STUNT LINE
TMC P/N
JJ333-9SRSI2
PLUG
TTY
EQUIPMENT
(0) (1)
+
-

SECTION III
OPERATOR'S SECTION

3-1. FUNCTIONAL OPERATION

a. General - The RTMU receives the coded teletype tuning command message from the remote operator and stores the code bits within its memory section. Upon receipt of the "tune" code from the remote operator, the RTMU energizes an associated equipment decoder. The energized decoder then proceeds to set up a reciprocating action with the RTMU whereby the codes are drawn out of the memory one-by-one. As each code is drawn out, the decoder alternately selects and positions an equipment control, as predetermined by the code pattern for that equipment. Memory capacity for an RTMU-41A is 32 codes, representing a control selection and a control positioning pair for 16 equipment controls.

At the beginning of each tuning command message there is an equipment selector (or "recognition") code. Each RTMU-41A is wired to respond only to one code or code combination. When the correct code arrives, (a letter-number combination) then RTMU opens its memory input in order to store the codes that follow. This arrangement allows a quantity of RTMU units to be fed from a single teletype channel.

A "clear" code from the remote operator at any time during the message will erase all code information out of the RTMU memory. This code is used to correct an error in the message. It is ineffective, however, unless received before the "tune" code, since the latter quickly precipitates the codes in the memory to the equipment controls via the decoder.

b. Five Single Equipment Systems - One RTMU-41A can control up to five single equipment systems, providing that each set has an individual decoder. In this mode, the remote operator sends an individual tuning message for each equipment properly prefixed with a letter (A through E) for the block of equipment controlled by the RTMU and a number (1 through 5) selecting the equipment within the block. This code also triggers a readback from the selected equipment.

c. Signal Input Indicator - (See figure 3-1.) A blinking of the front panel SIGNAL INPUT lamp indicates the presence of a coded teletype signal at that RTMU input. It does not indicate code storage, however. If an array of RTMU units is used, the local operator (or monitor checking out the remote-controlled equipment) should notice all RTMU units (fed by a common teletype channel) indicating a signal application while the code is being sent. Refer to table 3-1 for front panel control identification.

3-2. OPERATING PROCEDURES

Since the RTMU-41A functions only in a remote-controlled equipment application, there are no operating procedures, as such, for the RTMU-41A alone. Any one RTMU-41A can only store 32 codes in its memory (the equipment selector codes are not stored) in any one message. Any codes over 32 will not become stored and will therefore be ineffective. A "clear" code (if sent before the "tune" code) will erase all previous codes in a message and the corrected message may be repeated. When the "tune" code is sent, all the codes leave the RTMU memory one-by-one and act one-by-one on the equipment controls via the associated decoder driving these controls. Reciprocating action between the RTMU and the decoder ensures that a control has stopped moving (homed) before the next code is processed.

TABLE 3-1. FRONT PANEL CONTROL IDENTIFICATION

IDENT NO.	CONTROL NAME
1	ON/OFF Switch
2	POWER Indicator
3	SIGNAL INPUT Indicator
4	AC LINE Fuse
5	SPARE Fuse
6	AC LINE Fuse

3-3. OPERATOR'S MAINTENANCE

Local maintenance for the RTMU consists of an occasional inspection of fuses. Front panel AC LINE FUSES (see figure 3-1) are for instant notification of a short in the a-c power section. A light in the fuse holder cap indicates a blown fuse; a SPARE fuse holder with a spare fuse cartridge is located on the front panel. The power supply circuitry beyond the a-c input includes short-proof feature; therefore a short on a power supply output will not be injurious to any circuit component. Before replacing the fuse cartridge, pull out the RTMU on its drawer slides and inspect the POWER switch wiring and transformer for possible causes of short.

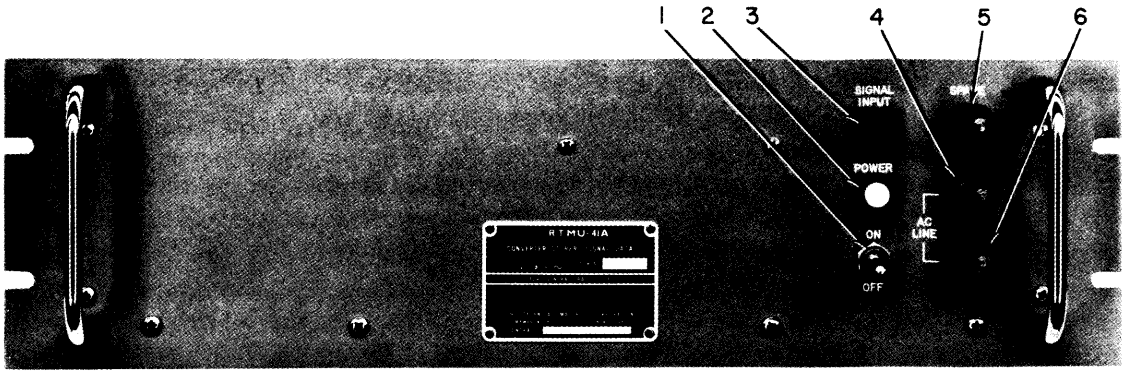


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Figure 3-1. Front Panel Controls

SECTION IV
TROUBLESHOOTING

4-1. LOGICAL TROUBLESHOOTING

a. Introduction - When adequate historical data on the type of trouble encountered by the operator is not available, there are four steps to be taken in logical troubleshooting procedure. These are:

Symptom recognition

Symptom elaboration

Listing probable faulty functional sections

Localizing malfunction to the faulty printed circuit card

Localizing faulty component on a circuit card.

b. Symptom Recognition - When it becomes noticeable that a function or a normal operation of the RTMU is not operating properly, a little functional analysis of the equipment system, before any corrective steps are started, will help localize the problem saving much time and effort. The technician should investigate the possibility that the difficulty could be from a source outside of the RTMU; i.e.: power or TTY line failure, decoder or equipment fault, etc.

c. Symptom Elaboration - After it has been determined that the RTMU is at fault, the symptom should be examined more closely. In order to bring the malfunction to a point where the trouble can be more clearly understood, the remote control station or local teletypewriter keyboard should be employed to further create those operational conditions, which will emphasize or increase the malfunction symptoms, to such a degree that the faulty stage of operation can be identified.

d. Listing Probable Faulty Functional Sections - The RTMU-41A divides into five functional sections (see paragraph 4-2b). With a knowledge of the symptoms, a reference to paragraph 4-2b should help in isolation to the faulty section or sections.

e. Localizing The Trouble to The Faulty Printed Circuit Card - Each functional section consists largely of plug-in type printed circuit cards. Spare plug-in cards, when available, are substituted for suspect cards to reduce troubleshooting time. When spares are not available, however, usage of the troubleshooting chart, table 5-2, should expedite fault isolation to the faulty card or assembly.

f. Localizing Faulty Component on Printed Circuit Card - Once the faulty card (or area) has been established, the final step is to repair it (or replace it with a card which is good). Faulty cards should be replaced if possible, not repaired, in order to expedite return of the RTMU to service. Faulty cards can be repaired using procedures in Section 5.

4-2. OVERALL FUNCTIONAL DESCRIPTION

a. Introduction - This section covers overall functioning of the RTMU-41A. The RTMU is constructed largely of printed circuit plug-in cards and assemblies shown in table 1-1. The functional servicing block diagram accompanying the following text is in terms of the functioning of individual cards and assemblies.

b. Functional Sections (figure 4-1)

(1) Code - Entry - Equipment tuning codes from the remote operator enter the equipment by way of isolation keyer card A1. The 5-bit binary codes are made up of pulses of current from a standard keyed teletype current loop and include a "start" pulse at the beginning and a "stop" pulse at the end. Isolation keyer card A1 keys a logic voltage in the input of clock timing card A2 and also serves to isolate the code inputs of an array of RTMU units working from a common teletype current loop.

Clock timing card A2 contains a decade counter circuit that functions as a shift-register with ten shifts per character. The "start" pulse triggers a clock in the register. The next five shifts move the first five bits of the character over to parallel shift-register A3. The next three shifts give the Converter-Storer the ability to accept transmissions of the 6, 7 or 8 level characters. The final shift is generated from pin E of A3 from a flip-flop (part of the decade-counter register in A2) and this serves to stop the clock in A2. The first five bits of the code become stored momentarily in the A3 register and move above, in parallel pulses, to the five bit-memory sections in integrated shift register A7. The codes cannot become stored in A7, however, until A7 receives a "memory input gate control" signal from Shift Tuning Circuit A6 (pin T).

The shift-register in card A3 is so arranged as to allow a time interval of 220 milliseconds or 135 milliseconds for the passage of each code corresponding with the time required for a standard 8-level transmission. This arrangement adapts the RTMU to work with an existing 8-level teletype linkage; however, the RTMU uses only the first five bits of the code.*

* In a manual keying, not to exceed 60 WPM.

The "memory input gate control" signal is also sent to pin N of A3 and operates a gate which allows the "1" bits of characters in the rest of the message to be sent to the "Bit Memory" on A7. At the same time, A6 releases an "equipment selected" signal to stunt relay K1, energizing it into its "correct" position. This extends a ground (or "stunt" signal) to each of the other four equipments on the common teletype line at pin 3 of A2, closing their respective code input gates. K1 also generates an "equipment selected" readback signal for that equipment.

With the bit-memory gates set open, the next code to arrive (the first tuning instructions code) becomes stored. The Shift Timing Circuit (A6) receives "clock pulses" on pin W and "single shift pulses" on pin X for each incoming character. These signals are sent to a gate in Z-11 which generates a "single shift" signal for each character. This signal causes the "Timer" to send a "shift pulse" to pin 6 of A7. The "shift pulse" moves the bits of the character in parallel by one position towards the "Bit Memory" output on A7. Each successive code is moved into the memory in this manner, moving towards the output to make room for the next code in the input. Maximum capacity of the bit memories is for 32 codes. This continues in this manner until the arrival of the "E" (or "equipment tune") code, at the end of the message.

(2) Code Monitoring - Card A3 and gating circuit card A4 serve to analyze the codes for three particular types of code: equipment selector, "clear", and "E" code. The equipment selector code is a 2-code combination at the beginning of the message that (via energized stunt relay K1) effectively unlocks the input to the RTMU memory for the rest of the codes in the tuning message. The "clear" code, if received any time during the message prior to the "E" code, will result in a "clear" pulse to the memory via shift timing circuit card A6, releasing existing codes out of the A7 bit memory section. The clear code (01111) produces a "clear" signal from pin 8 of A3 to pin 6 of A6. A6 then emits a series of fast shift pulses to the memory, moving the codes out of the bit memory on A7. Since no "E" has been sent, pin E of A7 does not produce the monitor signal back to A6 to shut off the shift pulses. However, when the next code is sent, the removal of the clear signal at pin 6 of A6 stops the pulses. Although the released codes move into the Decoder, there is no code transfer action since there is no "start tune" signal and, consequently, no tune lockup continuity established.

(3) E Code Entry - When the "E" code is received, it causes a "tune" signal to appear at pin 17 of A3. This signal is carried to pin 19 of A6 and A6 produces an "E" signal at pins S and 5. The output on pin 5 is not used in the RTMU-41A. The "E" signal on pin S sets a "monitor" gate in A7 and opens a "start tune" gate in A4. A "start tune" signal is then issued to the Decoder. At the same time, the "E" precipitates a series of "fast shift" pulses from pin V of A6 to the bit-memory sections in A7. This moves all the codes towards the output of the sections. When the first bit #1 arrives at A7 output, a "monitor" pulse is generated and travels through the monitor gate to pin J of A6, stopping the "fast shift" pulses.

It is at this point that the code storage phase is over; the arrival of the "start tune" signal at the Decoder and the five code bits at its input precipitate the next phase in which a reciprocating action (or code transfer) starts between the RTMU and the decoder: the code transfer phase.

(4) Code Transfer - The first code to enter the decoder causes the decoder to move a stepping switch to a prescribed position; when this happens, the decoder sends back another "memory advance" signal to card A6 and a "memory inhibit" signal to clock timing card A2. This latter signal remains during the entire transfer phase and prevents any succeeding remote tuning messages from entering the RTMU while the equipment is processing the current message. The second "memory advance" signal generates another "shift" signal from card A6 and this works on card A7 to shift out the next code. The cycle is repeated until all of the codes are drawn out of the RTMU. In each code transfer cycle, while the code is being transferred from the RTMU to the decoder, a "decoder inhibit" signal is issued to the decoder stepping switch power supply from card A6 preventing stepping switch movement.

(5) Readback Signals - Two readback signals issuing from the RTMU are for transmission back to the remote operator. One is the "equipment selected" signal that is generated by the energized stunt relay (K1), indicating that the RTMU memory has opened to the message. The other signal is a "memory power off" readback issuing from a sampling of the logic power supply voltage in clock timing circuit A2; this alerts the remote operator to the fact that the RTMU power has been turned off locally and that a remote tuning is not possible.

(6) Blank Code - In some types of teletype transmitting equipment, it is possible for the operator to inadvertently send a "blank" code. This is a "start" pulse, followed by five "0" bits (or absence of code). A blank (00000) code gate in A3, in this case, prevents this code from becoming stored in the memory. A "blank rej" signal output from pin 18 of A3 works through an inverter in A6 to inhibit the usual shift triggering pulse from pin V of A2 to pin X of A6. Since the preceding code into the memory has not been shifted, the blank code does not become stored.

c. Equipment Control - The RTMU-41A can control and has readback-selection of five equipments (via five decoders). Data from parallel shift-register card A3 is analyzed in gating circuit card A4 to determine which decoder, 1 through 5, is being addressed by the remote station. Card A4 has five separate "start tune" outputs, controlled by the equipment selector codes. The "start tune" signal is initiated and applied to the addressed decoder and signal data is generated for transmission to readback selector assembly, A11, to position the RTMU

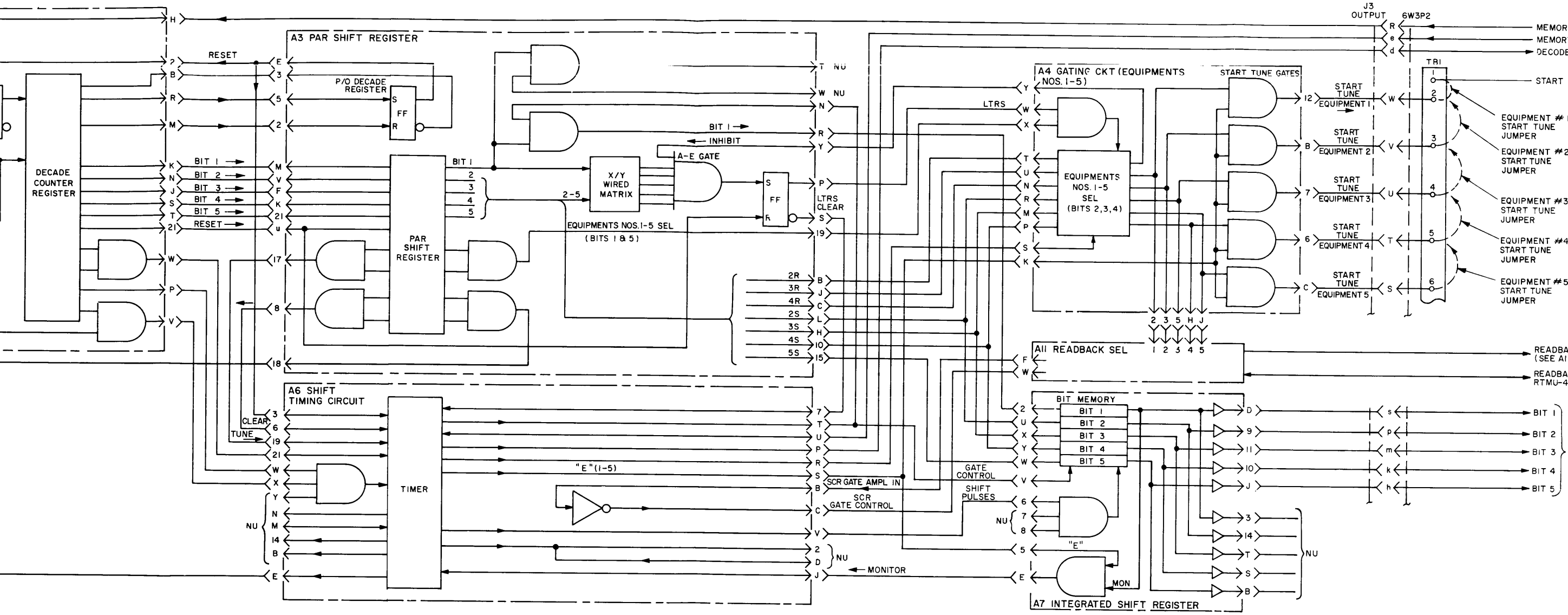
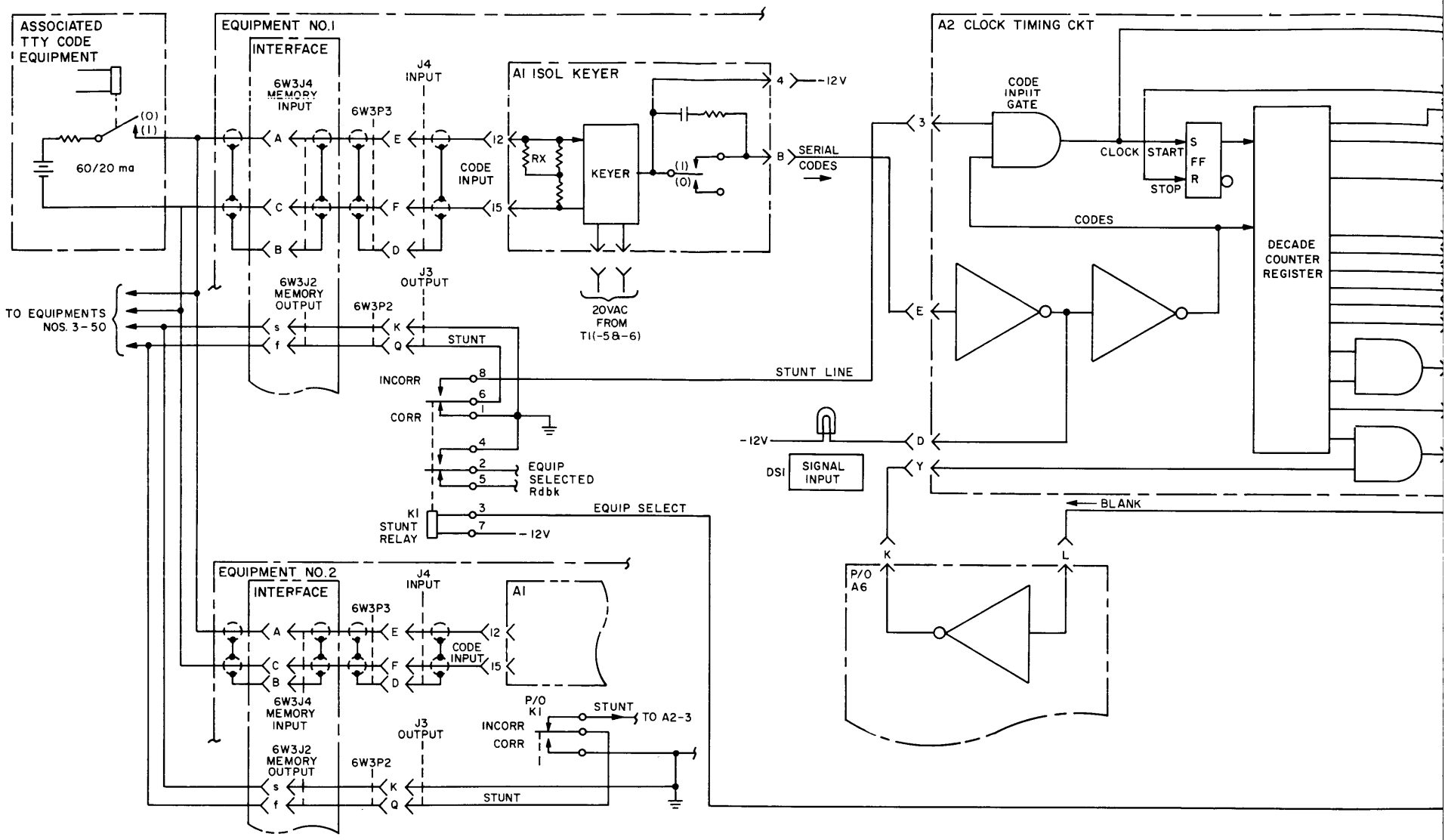


Figure 4-1. Functional Servicing Block Diagram


ASSOCIATED TTY CODE EQUIPMENT
(0)
(1)
60/20 ma
EQUIPMENT NO.1
INTERFACE
6W3J4 MEMORY INPUT
J4 INPUT
6W3P3
A
C
B
E
F
D
12
15
CODE INPUT
AI ISOL KEYER
RX
KEYER
4
-12V
B
SERIAL CODES
(1)
(0)
20VAC FROM T1(-5&-6)
TO EQUIPMENTS NOS. 3-50
6W3J2 MEMORY OUTPUT
J3 OUTPUT
6W3P2
s
f
K
Q
STUNT
INCORR
CORR
8
6
1
4
2
5
EQUIP SELECTED Rdbk
STUNT LINE
KI STUNT RELAY
3
7
-12V
EQUIP SELECT
A2 CLOCK TIMING CKT
CODE INPUT GATE
3
CLOCK START
STOP
S
FF
R
CODES
DECADE COUNTER REGISTER
E
-12V
D
DSI
SIGNAL INPUT
Y
BLANK
K
L
P/O A6
EQUIPMENT NO.2
INTERFACE
6W3J4 MEMORY INPUT
J4 INPUT
6W3P3
AI
A
C
B
E
F
D
12
15
CODE INPUT
6W3J2 MEMORY OUTPUT
J3 OUTPUT
6W3P2
s
f
K
Q
STUNT
P/O KI
INCORR
CORR
STUNT
TO A2-3

readback selector switch to the correct position for transmission of equipment common, mark and space readback data from the addressed decoder to the remote station. Readback selector assembly A11 is essentially a code-operated stepping switch, operated by a 1-5 equipment selector code and selects one of five decoder readback outputs for transmission back to the remote operator.

4-3. CIRCUIT CARD DESCRIPTION

This paragraph contains discussion of the 7 plug-in cards in the RTMU-41A. These discussions are to be used in conjunction with figures 4-1 and 7-1, the troubleshooting chart, table 5-2, and the specific schematic for the card under discussion when isolating RTMU-41A malfunctions to a defective card. Individual cards are discussed in paragraphs 4-3a through 4-3h. Table 4-1 is a listing of programming codes.

a. Isolation Keyer Card, A1 - (See figure 7-2.) Isolation keyer card, A1, is employed to change neutral or polar current inputs into negative serial voltage-code output signals. It is basically comprised of a transistor, dc power supply, a two-coil relay and functions as follows.

A positive input signal drives transistor Q1 into saturation and operates the normally-open coil of relay K1, which in turn applies -12 vdc through its normally open contacts to pin B.

TABLE 4-1. PROGRAMMING CODES

A. EQUIPMENT SELECTION

A - 10101 - Y	1 - 00010 - CR	NOTE: CCIT Codes
	2 - 01010 - R	
B - 10110 - F	3 - 01100 - I	CR - Carriage Return
	4 - 01000 - LF	
C - 11010 - J	5 - 00100 - SP	
	6 - 01101 - P	LF - Line Feed
D - 11001 - W	7 - 00101 - H	
	8 - 00011 - O	SP - Space
E - 10011 - B	9/A - 00111 - M	
	10/B - 01011 - G	

B. FUNCTIONS

1. Frequency Selection

10 Mc - 11000 - A	0 - 01000 - LF	5 - 00110 - N
1 Mc - 10100 - S	1 - 00100 - SP	6 - 01110 - C
100 Kc - 11100 - U	2 - 01100 - I	7 - 00001 - T
10 Kc - 10010 - D	3 - 00010 - CR	8 - 01001 - L
1 Kc - 11010 - J	4 - 01010 - R	9 - 00101 - H
0.1 Kc - 10110 - F		

2. CMRA - 4 MODE - 11110 - K

CW - 01000 - LF
Push to Talk - 00100 - SP
VOX - 01100 - I
Norm - 00010 - CR

3. Carrier Supression - 10001 - Z

0 db - 01000 - LF
3 db - 00100 - SP
6 db - 01100 - I
20 db - 00010 - CR
30 db - 01010 - R
Full - 00110 - N

4. Output Power - 11001 - W

1 - 01000 - LF	Full Power
2 - 00100 - SP	3/4 Power
3 - 01100 - I	1/2 Power
4 - 00010 - CR	1/4 Power

TABLE 4-1. PROGRAMMING CODES (Cont)

5. High Voltage - 10101 - Y	
	ON - 01000 - LF OFF - 00100 - SP
6. Fault Reset - 11101 - Q	
	Fault Reset - 01000 - LF
7. Tune - 10000 - E	
8. Clear - 01111 - V	

In the absence of an input signal, transistor Q1 ceases to conduct and de-energizes the normally-open coil of relay K1. The normally-closed coil of relay K1, which is connected so as to assure a relatively large current flow through it during nonconduction of Q1 and a small current through it when Q1 conducts, then energizes and causes the normally-open contacts to return to the open state.

Resistor R4 is adjustable and is normally adjusted to assure rapid, positive relay operation. Diodes CR1 and CR3 are employed to reduce or eliminate relay coil ringing. Refer to paragraph 2-5c7 for adjustment of R4.

b. Clock Timing Circuit Card, A2 - (See figure 7-3.) The greater part of the circuitry in the clock timing circuit is used in the equipment's remote tuning section. Input code signals enter the clock timing circuit on pin E. The signals are fed through inverter Z8 to pin D to activate the SIGNAL INPUT indicator and through an additional inverter Z8 to two AND gates in Z4. In the absence of a "stunt" signal, from pin 3, a "start" pulse input to Z4 creates an output from Z4, (pin 10) which sets flip-flop Z1 to start time generator Z2. Z2 then commences to issue a series of regular pulses at pin 6 and at pin 11. The output of Z2 (pin 11) is applied through ss generator Z3 to AND gate Z4. When the signal from Z3 is coincident in time with the signal from Z8, this Z4 gate is enabled and creates a master timing signal at pin 11 which is applied to AND gates in Z5, Z6 and Z7. The output of Z2 (pin 6) is also applied to flip-flop Z11 and to emitter follower Z12. The output of flip-flop Z11 is applied through AND gate Z4 and flip-flop binary Z9/Z10 to AND gates Z5 and Z6 which, in conjunction with the master timing signal from Z4 - pin 11, enable gates Z5, Z6 and Z7 and generate: bit 1 through bit 5 output pulses which are applied to pins K, N, J, S and T respectively; the 'tune FF set' pulse which is applied to pin W; and the 'common reset' pulse which is applied to pin 21. The Z4 AND gate which controls Z9/Z10 is enabled by the '4th FF reset out' signal which enters the card on pin B.

The output of emitter follower Z12 (bit shifting pulses for external memory register) is connected to pin P.

Outputs of flip-flops Z9 and Z10 are also applied to an AND gate in Z7 to produce the 'single shift pulse' when coincident in time with the blank reject pulse which enters card A2 on pin Y. Outputs of flip-flops Z11 and Z10 are also used as '1st FF binary reg' and '3rd FF binary reg' signals.

The -12 vdc which enters on pin F is inverted in Z8 to create the 'memory power off' signal.

c. Parallel Shift-Register Card, A3 - (See figure 7-4.) Parallel shift-register card A3 is utilized to change the serial digital data from card A2 into parallel data and to generate system control signals.

Serial digital data enters card A3 on pins M, V, F, K and 21 and is stored in flip-flops Z2 through Z6 until they are reset by the common reset pulse which enters the card on pin U. Data stored in Z2 through Z6 is selectively applied: to AND gate Z11 to generate the 'Sel 1-5' signal which is applied to pin 19; to AND gates Z9 and Z11 to generate the 'blank rej', 'tune E' and 'memory clear' signals which are applied to pins 18, 17 and 8 respectively; the AND gate Z10 which, in conjunction with an enable 'memory A input gate control' signal (which enters the card on pin N), generates the 'Bit 1 A memory' signal which is applied to pin R; to AND gates Z7 and Z10 to generate the 'ltrs memory clear' signal which is applied to pin S; to AND gate Z7, flip-flop Z1, and AND gate Z10 to generate the 'gate enable' signal which is applied to pin P. The 'ltrs gate inhibit' signal from pin Y is an input to AND gate Z7 in the generation of the 'gate enable' and 'ltrs memory clear' signals. AND gate Z7, together with a specially wired X/Y matrix opens to the correct selector code when not inhibited by an inhibit signal on pin Y.

Flip-flops Z3, Z4, Z5 and Z6 also apply parallel digital data to pins L, B, H, J, 10, C, 15 and J.

Flip-flop Z8 is set by the '3rd FF binary reg' and reset by the '1st FF binary reg' signals which enter card A3 on pins 5 and 2 respectively. The '4th FF set out' and '4th FF reset out' signals of Z8 are applied to pins E and 3 respectively.

d. Gating Circuit Card, A4 - (See figure 7-5.) Gating circuit card A4 is used to generate the five 'start tune', the five 'readback select out' and the 'ltrs gate inhibit' signals.

Bit 2, 3, and 4 of the equipment selection code set and reset signals, which enter the card on pins M, N, P, R, T and U, are applied in conjunction with the 'sel 1-5' and ' gate enable (1-10)' signals which enter the card on pins X and W respectively, to AND gates Z10 and Z11 for decoder and readback selection. The 'gate enable (1-10)' and 'sel 1-5' signals are applied to an AND gate in Z7. The output of this AND gate is applied through two inverters in Z6 to act as a release pulse for the Z10 and Z11 gates. A signal from Z10 and Z11 is applied to set flip-flop Z1, Z2, Z3, Z4 or Z5. These flip-flops serve as storage devices for signals used in the generation of 'readback select', 'start tune' and 'ltrs gate inhibit' signals.

Upon receipt of a decoder number (1 through 5) the corresponding flip-flop (1 through 5, respectively) will be set and will remain in the set state until reset by the 'E or clear reset' signal which enters the card on pin S and is inverted in Z6. During this 'set' time, one of the inputs to an AND gate in Z7 (with an extended input from Z1, CR6) will be in the '0' state. The resultant output of the AND-complex will be a '0' which is applied to pin Y as a 'ltrs gate inhibit' signal. When no decoder has been selected the signal on pin Y becomes a '1'. During set period, the output of the set flip-flop will be applied to an AND gate which is comprised of CR7, CR8 and R3 or to an AND gate in Z9. The outputs of these AND gates are fed through inverters in Z6 and Z8 to pins 12, B, 7, 6 or C for application as 'start tune' signals to decoders 1 through 5 respectively.

The 'E or clear reset' signal entering at pin S is applied through inverter Z6 to flip-flops Z1 through Z5.

The set outputs of flip-flops Z1 through Z5, which represent the number of the selected decoder, are also applied through diodes, CR3, CR4, CR5, CR1 and CR2 as 'readback select out' signals to pins 2, 3, 5, H and J respectively.

e. Shift Timing Circuit Card, A6 - (See figure 7-6.) Card A6 is used to generate signals which control the sequencing through the rest of the remote tuning circuit. Timing generator Z1 is for pacing a "fast-shift" in the memory section; this occurs after the "E" has been received and the code bits in the associated memory storage are being shifted towards the output, after a 'clear' has been received to shift codes out of memory, and during the first character of a message to fast-shift any previously existing codes out of memory. Timing generator Z2 generates the "single shift" into the memory in the reciprocating signals that occur during code transfer into the associated decoder. Both timing generators work (Z2 works via Z3 inverter output pin 9) through an AND gate (with output pin 11) in Z5 and an inverter in Z3 (output pin 11) to fire single-shot Z7, producing the negative 2-microsecond shift pulses required. In the initial phase in which the codes are becoming stored in the memory, pulses from an external timing generator, entering at pin W, and a set signal via pin X, travel through an AND gate in Z11 (with output pin 6) and an inverter in Z9 (output pin 7) and serve as the memory bit shift pulses. These also take the common path through Z5 AND gate, Z3 inverter, and single-shot Z7. Enabling timing generator Z2 are two signals: (1) the "E" signal entering at pin 19 working through an AND gate (with output pin 11) in Z11 and the set for that gate at pin 21 and flip-flop Z8 to diode CR4 and (2) the "memory advance" signal entering via pin U and brought to diode CR3. Diodes CR3 and CR4 form an AND gate in such a way that the signal entering via pin U will pass through the gate and to Z3 inverter (output pin 7) except during the time that the gate is inhibited by the tune signal (pin 19, via Z11 output pin 11 and Z8). The output of Z8 (pin 6) is also applied through Z10 (with output pin 6) to pin S as an 'E out' signal. The signals on pin 7 of Z3 will trigger the timing generator Z2 to produce single pulses. There are three signals enabling timing generator Z1: (1) "letters gate clear" signal which occurs during the first character of a program (pin 7 via Z9 inverter output pin 11), (2) "bit 1 'A' monitor" signal via pin J and (3) a "clear" signal which occurs only during the program input of a "clear" character (pin 6 via Z9 inverter, output pin 6, and Z10 amplifier, output pin 11). Either the "letters gate clear" or the "clear" signal will trigger the timing generator Z1 via Z4 inverter (output pin 7) to produce a series of fast shift pulses (30kc). The "bit 'A' monitor" signal (pin J) will inhibit AND gate Z5 (output pin 6) during the tuning process as soon as the first "1" bit comes out of memory.

Signal inputs on pins D, 3, 6, 19 and 21 are required for the generation of the "Memory 'A' input gate control" signal on output pin T. The 'memory clear' signal on pin 6 is applied through inverter Z9 (with output on pin 6) and emitter follower Z10 (with output on pin 11) to pin 8 of an AND gate in Z6. When the 'memory clear' signal is '0', an enable signal '1' is applied to Z6. (A '0' on pin 6 is inverted to a '1' by Z9 and applied through Z10 as a '1' to AND gate Z6). The other input to Z6 (pin 1) is derived from the reset output of flip-flop Z8. When either input to pins 9 or 12 of AND gate Z11 is '0', or when the input to pin 3 is a '1', Z8 is not set and a '1' is applied to pin 1 to enable AND gate Z6. The output of this AND gate (pin 10) is applied to pin 3 of another gate in Z6. The 'ltrs gate inhibit' signal from pin D is applied through inverter Z4 and diode CR2 to pin 3 of Z6. When the input on pin D is '0', (non-inhibit), the 'memory A input gate control signal output on pin T not affected; when the input on pin D is a '1' (inhibit) the anode of diode CR2 is grounded and any '1's from pin 10 of Z6 are grounded through CR2 resulting in a '0' on pin T.

The 'control (equip select)' signal is generated by the input on pin D. A '1' input is inverted in Z4

to a '0' which is applied through another inverter in Z4 to pin E. The output of this inverter is a '1' which has no effect on the operation of shunt relay K1. When the input on pin D is a '0', the double inversion in Z4 places a '0' (ground) on stunt relay K1 which applies a bias to card A2 preventing entry of information into the system.

With the exception of the input signal on pin D, the same digital logic utilized in the generation of the 'memory A input gate control' signal is used in the generation of the 'E or clear reset' signal on pin R.

In the RTMU-41A only the Z6 gate with output pin 6 is used; in other RTMU's (dual memory type), this gate is used for the "A" memory and the other (output pin 5) is used for the "B" memory. Z9 (output pin 9) inverts the incoming signal on pin L to produce the "blank reject" signal (pin K). Z4 (output pin 11) inverter is not used in the RTMU-41A. Z3 inverter (output pin 6) produces the "decoder inhibit" signal (pin P). A "letters gate inhibit" signal enters on pin D and is inverted by Z4 (output pin 6). This inverted output leaves the card on pin 2; however, this signal is not used in the RTMU-41A. The signal at Z4 (pin 6) is also routed to a second inverter (Z4 output pin 9) and to CR2.

f. Integrated Shift-Register Card, A7 - (See figure 7-7.) Integrated shift-register card A7 is used as the store and forward device of the RTMU. Signal data enters this card on pins U, X, Y, and W. The data on these pins is shifted through AND gates in Z11, by a 'memory A input gate control' on pin V, to shift registers Z2, Z3, Z4 and Z5 respectively. Data is stored in the shift registers until receipt of the 'memory A shift in' pulse which enters the card on pin 6. This 'shift' pulse is applied through a buffer in Z6 to each of the shift registers. Receipt of the shift pulse transfers the data, one code at a time, from the shift registers through inverters in Z7 to another set of inverters in Z9. The 'bit 1 A mem' signal on pin 2 is routed through shift register Z1 by the 'shift pulse' to an inverter in Z8. The output of the inverter is applied to pin 4 of AND gate Z6. When the signal on Z6 pin 4 is time coincident with the 'E out' signal on pin 5, a '1' is applied to pin 1 of inverter Z8. The output of this inverter is applied as a 'bit 1 monitor' signal to pin E. This signal shuts off the fast-shift on card A6 when the first bit 1 comes out of memory, and also gives bit 1 information on pins D 'bit 1 (SGL & dual A1-5)' and 3 (not used).

Equivalent outputs to the signals on pins D, 9, 11, 10 and J (which are not used in the RTMU-41A system) are on pins 3, 14, T, S and 13 respectively. The output on pin 3 is derived through an inverter in Z8; the outputs on pins 14, T, S and 13 are from inverter Z10.

g. Power Supply Card, A10 - (See figure 7-8.) Power supply card A10 contains the +12 VDC, -12 VDC and -27 VDC supplies which are used to power the RTMU circuitry. Both the -27V and +12V regulators are completely contained on this card. The -12V supply has its rectifier, filter capacitor and a control transistor chassis-mounted, external to this card. Input to each of the 12V supplies is 18 VAC from one of the secondary windings of power transformer T1.

Because both sections are quite similar in operation, only the +12 VDC section need be fully explained; the differences between the +12 VDC and -12 VDC will also be noted.

Incoming AC (pins 16 and 17) is rectified by full-wave bridge rectifier CR2, and passes through a surge limiter consisting of R29. The resultant pulsating DC is applied to pin 3 of Z3: Z3 is an integrated voltage regulator, incorporating current limiting and short-circuit overload protection. Essentially, Z3 functions as an operational amplifier with heavy feedback.

An output of Z3 is applied to the base of driver Q5; Q5, along with R11, forms a divider-bias network for series-pass transistor Q4, which performs the actual regulation: Q4's collector-emitter path falls in series with the filtered output of CR2 (filtering is accomplished external to A10 by capacitor C2 connected between board pin V and ground). Q4 thus acts as a series resistance, varied by Z3, via Q5. Therefore, voltage output is ultimately regulated by Z3. To regulate properly, however, Z3 must have an error input: this input is obtained by sampling the output voltage at the junction of the voltage divider formed by R23 and R25. The error sample is applied as feedback input to terminal 6 of Z3 (for the reader's information: within Z3, the error input is compared with an internal voltage reference standard in what amounts to a differential amplifier; output of this amplifier is applied to the base of Q5). Capacitor C6, connected between terminals 6 and 7 of Z3 is part of an internal frequency compensation network, to prevent oscillation at high frequencies and/or transient "ringing". Capacitor C7 bypasses stray pickup, and resistor R26 is an output bleeder. Resistor R28 and capacitor C5 are part of the DC reset line, to be discussed shortly.

Current limiting is accomplished by Z3 in conjunction with resistors R24, R12 and R13; limiting of the "switchback" type, i.e.-when a heavy current overload occurs, the switchback limiter reduces current flow to a relatively small fraction of maximum output, instead of simply limiting current flow to the maximum design value, until the overload is removed.

Limiter operation is as follows: Output current creates a voltage drop across R24, which would appear between Z3 terminals 1 and 8; however, the divider composed of R12 and R13 causes another voltage drop; this drop bucks out the drop across R24. It is this bucking action which allows the above-mentioned current increase (in this case, maximum load current is on the order of 2.0 amperes). However, consider the case of a short circuit at the output: R12 and R13 are effectively in parallel

across the output; therefore, the voltage across the combination approaches zero, and the bucking voltage is no longer generated. The heavy current through R24 causes a relatively large drop to appear between Z3 terminals 1 and 8: these become the current-limiting input terminals. Z3 immediately reacts by reducing forward bias on Q4 until output current returns to a safe predetermined value (in this case, about 0.5 amp). The combination of R12 and R13 also provides a pre-load on the output of about 20 ma, so the regulator will always operate into a load of some sort.

Z3 terminal 4 is ground input for the IC; terminal 5 of Z3 is connected to ground through bypass capacitor C9. C9 reduces noise in the internal voltage reference source by the usual bypass action.

The -12 volt section of A10 functions in an identical manner to the +12-volt section, with the following exceptions: the -12 VDC series-pass transistor (Q1) is mounted external to the board at pins U (emitter), N (collector), and 13 (base). The full wave bridge rectifier CR2 is also mounted external to board A10; its input to A10 are: negative voltage on pins H and J; positive voltage on pin N. The surge limiter comprises resistors R19, -20 and -22. Due to the polarity inversion, the current limiter bucking divider is connected between the surge limiter network and the junction of R27 and R9.

The -27 volt section of A10 also functions in an identical manner to the +12 volt section.

Resistors R6 and R28, and capacitor C5, form the DC Reset circuit. The purpose of this circuit is to reset both Gating Circuit A4 and Shift Register A3 to a CLEAR (no code entry, clock stopped, shift register "zeroed") condition, upon initial application of power to the unit.

R6 and R28 are in series between +12 VDC and -12 VDC board output, thereby forming a voltage divider across which is impressed 24 VDC. The resistances are in a ratio of 2.225 to 1.00, favoring the -12 VDC leg; therefore, the DC Reset line, taken from R6 -R28 junction is held approximately 8 volts above -12 VDC, or about -4 VDC with respect to ground.

Note, however, that R28 is shunted by C5. Upon initial power application, C5 presents a very low DC resistance until it charges, effectively short-circuiting R28, and immediately raising the DC Reset line to +12 VDC. This positive-going pulse is used to reset the shift register and clock gating circuits, thus correcting any spurious triggering caused by initial power surges. As C5 charges, its DC resistance quickly rises to a nearly infinite value, effectively removing the short circuit from R28, and allowing the Reset line voltage to fall back to -4 VDC, thus locking out the DC Reset line until the equipment is shut down, then once more reactivated. DC Reset is accomplished in approximately the first 100 milliseconds after power application.

h. Readback Selector Card A11 - (See figure 7-9.) Readback Selector Card A11 is used to connect the readback data lines of a remotely selected decoder to the remote station lines. Card A11 is basically comprised of a stepping switch and an SCR.

Decoder-selected inputs enter card A11 on pins 1 through 5 for decoders 1 through 5 respectively. Assume, for example, decoder 3 has been addressed by the remote station. A '1', from card A4, enters card A11 on pin 3. The '1' is applied to contact 3 on S1. If S1 is in any position, other than position 3, the '1' is applied through the wiper of S1 via pin F to an inverter which is located on card A6. The output of the inverter, '0', is applied, via pin W on card A11, to the SCR. The SCR will energize the stepping switch until it rotates into position 3, at which time the wiper arm of S1 will present its open contact to pin 3; the SCR will turn-off and S1 will cease to rotate. The space, common and mark wafers of S1 will now be in position to accept readback data from decoder 3 for routing to the remote station.

SECTION V
MAINTENANCE

5-1. PREVENTIVE MAINTENANCE

The following paragraphs describe procedures for inspecting, checking and cleaning the components of the RTMU-41A. In general, preventive maintenance provides a basis for recognizing future probable causes of equipment malfunction in the early stages of deterioration. Many such causes are apparent to the senses of sight, touch and smell. Therefore, by adhering to a stringent program of preventive maintenance involving periodic inspection and checks, the most probable causes of equipment malfunction can be avoided, thereby minimizing equipment down-time and the possibility of compromising important schedules.

a. Inspection And Test - The following paragraphs describe equipment inspection and power supply checks to be performed on a weekly basis.

(1) General Inspection. A thorough visual inspection of an assembly or component for signs of deterioration prior to failure can save test and troubleshooting time resulting from a complete breakdown. Table 5-1 presents a weekly inspection checklist for the RTMU-41A.

TABLE 5-1. WEEKLY INSPECTION ROUTINE

Assembly or Subassembly	Check
Line Power Cord	Check three-wire line power cord for cracks, nicks or fraying
Main Chassis Assemblies	1. Check underside of chassis for dirt and dust
	2. Check all inter-connector wiring for nicks, cracks or fraying.
	3. Check all printed circuit boards for cracks; check components for looseness and evidence of deterioration from possible overheating.
	4. Check printed circuit board jacks for tightness against chassis.
	5. Check ground connections for security.
Front and Rear Panels	1. Check panel for general cleanliness.
	2. Check Power ON OFF switch for positive action.
	3. Check indicator faces for cracks.
	4. Remove line fuses and check for proper 1-ampere or 0.5-ampere value and condition (0.5-ampere with 230 vac line).
	5. Check jacks J1 thru J4 for security against panel.

(2) Power Supply checks. Perform the following power supply routine maintenance as outlined in Section 2, paragraph 2-5c.

(3) Functional Test. Perform the checkout procedure for the RTMU-41A as outlined in Section 2, paragraph 2-5d.

b. Cleaning Instructions - In general, the RTMU-41A should be cleaned once a week, using a soft camel's hair brush, forced air pressure of not more than 20 psi and a suitable cleaning agent such as trichlorethylene or methylchloroform.

WARNING

When using toxic solvents, make certain that adequate ventilation is provided; prolonged or repeated breathing of the vapor should be avoided. Avoid prolonged or repeated contact with the skin. Flammable solvents shall not be used on energized equipment or near other equipment from which a spark may be received.

CAUTION

Trichlorethylene contains a paint removing solvent; avoid contact with painted surfaces.

Remove dirt or grease from wiring and chassis surfaces using cleaning solvent; dry with compressed air. Remove dust from printed circuit boards using a soft camel's hair brush. Blow out accumulated dust from inaccessible areas of chassis using forced air.

5-2. TROUBLESHOOTING

Circuits of the RTMU-41A are contained on 8 PC cards accessible from the top of the chassis. Some power supply components are mounted on the chassis and the blower is mounted on the rear wall of the chassis.

In general, malfunction of the RTMU will usually manifest itself by lack of or improper tuning commands to the controlled equipment. These malfunctions can be rapidly localized to a particular PC card by the process of logical elimination. By usage of a spare set of PC cards, troubleshooting can be facilitated by the board substitution method. Table 5-2 presents a major troubleshooting chart for the RTMU-41A which is used to isolate a malfunction to a card. Table 5-3 through 5-10 are troubleshooting tables to be used in isolating a malfunction on a card to a replaceable component.

TABLE 5-2. TROUBLESHOOTING CHART

Step	Trouble	Probable Cause	Remedy/Procedure
1	POWER indicator on front panel not lit.	Power transformer POWER switch or blower defective.	Observe AC LINE indicators on front panel. Perform step 2 or 7.
2	AC LINE Indicator's in step 1 not lit.	POWER switch, S1, power transformer, T1, defective.	Observe blower operation. Proceed to step 3 or 4.
3	Blower operating in step 2.	POWER indicator lamp or power transformer defective.	Replace POWER indicator lamp. If POWER indicator still not lit, replace power transformer, T1.
4	Blower not operating in step 2.	POWER switch, powerline - filter defective.	Check for AC line voltage between POWER switch wiper contacts and between the ON contacts with switch in ON position. Proceed to step 5 or 6.
5	AC line voltage measured between wiper contacts in step 4, but not between ON contacts.	Power switch failure.	Replace POWER switch and proceed to step 8.
6	No AC line voltage measured in step 4 between wiper contacts.	Powerline-filter failure.	Disconnect AC input connector, J1 and determine, by resistance measurement, which line filter is open; replace same, reconnect J1 to AC line voltage, turn RTMU ON and proceed to step 8.
7	AC LINE indicator(s) in step 1 is lit.	Short circuit or excessive load.	Examine chassis wiring for possibility of a short. Remove blower leads from TB1 and cards A1 and A10; replace fuses and turn on power. If fuse(s) blows, replace diode bridge CR2. If fuse still blows, replace power transformer T1. If fuse does not blow after removal of blower and cards A1 and A10 reinsert card A1. If fuse blows, troubleshoot card A1 using table 5-3. If fuse does not blow, insert card A10. If fuse blows troubleshoot card A10 using

Table 5-2. Troubleshooting Chart (Continued)

Step	Trouble	Probable Cause	Remedy/Procedure
7 (cont)			table 5-9. If fuse does not blow, replace blower. Proceed to step 8.
8			Send the letters R and Y. On receipt of message observe SIGNAL INPUT indicator blinking. Proceed to step 9 or 10.
9	SIGNAL INPUT indicator blinking in step 8.	Data is being received.	Proceed to step 14.
10	SIGNAL INPUT indicator not blinking in step 8.	SIGNAL INPUT lamp or card A2 defective.	Check TP2 on card A2 for negative pulses as letters Y and R are being sent. (Refer to Timing Chart for A2 card.) Proceed to step 11 or 12.
11	Pulses observed in step 10.	SIGNAL INPUT lamp is defective.	Replace SIGNAL INPUT lamp. Proceed to step 14.
12	No pulses observed in step 10.	Card A2 defective.	Insert an extender card between card A2 and its socket (XA2) and check for negative pulses at pin E of extender card as letters Y and R are being sent. If pulses observed, troubleshoot card A2 using table 5-4. If no pulses observed, proceed to step 13.
13	No pulses observed in step 12.	Power or signal input to card A1 missing or card A1 defective.	Remove extender card and insert card A2 into socket XA2. Insert extender card between card A1 and its socket (XA1). Troubleshoot card A1 using table 5-3.
14			Repeat message as required while performing step 15.
15	Equipment tuning commands not as sent.	RTMU or decoder defective.	Observe data on pins 9, 10, 11 and J of card A7. Proceed to steps 16 and/or 23 if observed data is same as sent; step 18, 19, 20 and/or 24 if no data is observed; step 18 if observed data is not the same as sent.
16	Data for step 15 is same as sent.	Decoder defective.	Troubleshoot card A7 using table 5-8. If equipment commands still not correct, perform step 17.
17		Card A4 or decoder defective.	Insert extender card between card A4 and its socket XA4. Send letters Y, R and E. Observe pin B, C, 6, 7 or 12, as applicable, for the negative 'start tune' pulse as the letter E is being sent. If pulse not present, troubleshoot card A4 using table 5-6. If pulse is present, problem is probably in decoder; troubleshoot same.

Table 5-2. Troubleshooting Chart (Continued)

Step	Trouble	Probable Cause	Remedy/Procedure
18		Card A7 defective.	Troubleshoot card A7 using table 5-8. Repeat step 14.
19	'Memory 'A' input gate control', 'memory 'A' shift in' or 'E out' pulse missing.	Card A6 defective.	Troubleshoot card A6 pins T, V, and S using table 5-7. Repeat step 14.
20	'Bit 1 'A' memory' or 'Bit 2 (set out)' pulse missing.	Card A3 defective.	Troubleshoot card A3 pins R and L using table 5-5. Repeat step 14.
21	Bit inputs to card A7 not as sent.	Defective PC card A2, A3, A4, A6, A10.	Insert extender card between card A3 and its socket (XA3). Observe pins M, V, F, K, and 21 on extender card for 5 usec wide pulses as Y's and R's are being sent. Proceed to step 22 or 23.
22	Pulse data in step 21 not same as sent.	Card A2 defective.	Troubleshoot card A2 using table 5-4. Repeat step 14.
23	Data observed in step 15 or 21 same as sent.	Card A3 defective.	Troubleshoot card A3 using table 5-5. Repeat step 14.
24	No data observed in step 15.	1. No 'start tune' signal.	Proceed to step 25.
		2. No 'memory advance' signal from decoder.	Proceed to step 26.
		3. No bit 1 to decoder.	Proceed to step 27.
		4. Relay K1 energized.	Proceed to step 28.
25	No 'start tune' signal to decoder.	Card A3, A4 or A6 defective.	Insert extender card between card A4 and its socket XA4. Send letters Y, R and E. Observe pins B, C, 6, 7 or 12, as applicable, for the 'start tune' pulse as the E is being sent. If no signal observed troubleshoot card A6 using table 5-7 and repeat observation. If still no signal, troubleshoot card A3 using table 5-5 and repeat observation. If no signal present, proceed to step 26. If signal is present, repeat step 14.
26		No 'memory advance' signal from decoder.	Remove extender card from card A7 circuit and insert it between card A6 and its socket, XA6. Send letters Y, R and E. Observe pin U as the E is being sent. If signal is present, troubleshoot card A6 using table 5-7 and repeat step 14. If no signal present, problem is probably in decoder. Troubleshoot same.

Table 5-2. Troubleshooting Chart (Continued)

Step	Trouble	Probable Cause	Remedy/Procedure
27		No 'bit 1' transfer to decoder.	Remove extender card from card A4 circuit and insert it between card A7 and its socket XA7. Send letters Y, R and E and observe pin U as the E is being sent. If signal is present, proceed to step 28. If signal not present, troubleshoot card A7 using table 5-8 and repeat step 14.
28		Relay K1 energized.	Insert extender card between card A6 and its socket, XA6. Send letters Y, R and E and observe pin E for a signal as the E is being sent. If signal is observed, problem is probably in the decoder. Troubleshoot same. If no signal is observed on pin E, troubleshoot card A6 Pin E using table 5-7.
29	Wrong decoder readback.	Card A4, A6 or A11 defective.	Insert extender card between card A11 and its socket XA11. Send letters Y, R and E. Observe signal on pin 1, 2, 3, 4 or 5 for decoder 1, 2, 3, 4, or 5 respectively as the letter E is being sent. If no signal present, perform step 30. If signal is present, perform step 31.
30	No signal observed in step 29.	Card A4 defective.	Troubleshoot card A4, pin 2, 3, 5, H or J (for decoder 1, 2, 3, 4, or 5 respectively) using table 5-6.
31	Signal observed in step 29.	Card A6 or A11 defective.	Observe pin W for signal on receipt of letter E. If no signal observed, troubleshoot card A6-pins B and C using table 5-7. If signal is observed, troubleshoot card A11 using table 5-10.

TABLE 5-3. ISOLATION KEYER CARD A1, TROUBLESHOOTING

Step	Trouble	Probable Cause	Remedy
1	No input codes received by clock timing circuit card A2 (0 volts).	Isolation keyer card A1 defective, or no external signal being received.	Insert extender card between card A1 and its socket XA1. Send letter R. Repeat letter R as required while performing steps 2 and/or 3.
2		No external signal being received.	Observe signal between pins 12(+) and 15(-) as the letter R is being sent. If no signal observed, troubleshoot TTY keyboard circuitry.

Table 5-3. Isolation Keyer Card A1, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
3		Isolation keyer card A1 defective.	Observe pin B for presence of signal as the letter R is being sent.
4	Constant voltage output on pin B.	Transistor Q1 or relay K1 defective.	If signal on pin B is a constant -12 vdc, replace transistor Q1. If signal still a constant -12 vdc, replace relay K1.
5	No voltage output on pin B.	Rectifier CR4 defective or signal from power transformer T1 missing.	If no signal appears on pin B, measure dc voltage output of rectifier CR4.
6		Defective rectifier CR4.	If voltage is zero, observe 20 VAC between pins W and X. If voltage is zero, replace transformer T1; if 20 VAC is measured, replace rectifier CR4.
7		Defective resistor R2 or capacitor C2, C3.	If voltage is measured on output of rectifier and not across capacitor C2, verify condition of capacitors C2 and C3 and if good, replace R2. If capacitor(s) defective, replace defective capacitor(s) and resistor R2. If output voltage still zero, replace transistor Q1 and/or relay K1 as required.

TABLE 5-4. CLOCK TIMING CIRCUIT CARD A2, TROUBLESHOOTING

Step	Trouble	Probable Cause	Remedy
1	Signal from card A2 defective.	Defective component in card A2.	Insert extender card between card A2 and its socket XA2. Send letters Y and R while observing each following step.
2	No data on pin P; data on TP6.	Z12 defective.	Replace emitter follower Z12.
3	No data on pins V and T; data on pin 21.	Z6 defective.	Replace digital AND gate Z6.
4	No data on pin V; data on pin T as the letter R is being sent.	No input signal on pin Y, or Z7 defective.	Verify signal on pin Y in accord with timing chart figure 5-3 as letter R is being sent. If in accord, replace digital AND gate Z7. If not in accord, replace digital inverter Z9 on shift timing circuit card A6.
5	No data on pin 21; data on pin W.	Z7 defective.	Replace digital AND gate Z7.

Table 5-4. Clock Timing Circuit Card A2, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
6	No data on pins J, K, N, S, T and W as letters Y and R are being sent.	Z3 or Z4 defective.	Sequentially observe signals on TP9, 13 and 7 for data in accordance with timing chart figure 5-3 as letters Y and R are being sent. If any signal not per figure 5-3, replace unit which test point samples.
7	No data on pins J, K, M, N, R, S, T, V, W, 21.	Z11 defective.	Replace digital flip-flop Z11.
8	No data on pins J, K, N, R, S, T, V, W, 21 as letters Y and R are being sent.	Z4 or Z9 defective.	Verify signal on test point 1 in accord with timing chart figure 5-3 as letters Y and R are being sent. If in accord, replace flip-flop Z9. If not in accord, replace AND gate Z4.
9	Output data on pin 7 only as letters Y and R are being sent.	Z1, Z2, Z4, Z8 or card A1 defective.	Observe pin E for data in accord with timing chart figure 5-3-TP2 as letters Y and R are being sent. If data not per figure 5-3, troubleshoot card A1 per table 5-3. If data is per figure 5-3, sequentially observe data on pin D (inverse of data on pin E), test points 2 and 3, pin 2, test points 4 and 9 for data in accord with figure 5-3. If data not in accord with figure 5-3, replace unit which test point, or pin, samples.
10	No ground on pin 7; -12 vdc on pin F.	Z8 defective.	Replace inverter Z8.

TABLE 5-5. PARALLEL SHIFT-REGISTER CARD A3, TROUBLESHOOTING

Step	Trouble	Probable Cause	Remedy
1	Data received at decoder not as sent.	Flip-flop Z2, Z3, Z4, Z5 or Z6 defective; or a bit input signal is defective.	Insert extender card between card A3 and its socket XA3. Proceed to step 2, 3, 4, 5, 6, 7 or 8 as required.
2		Input signal defective for bit 1, 3 or 5.	Send the letter "Y" and observe pins M, F and 21 for conformance with timing chart figure 5-4. If data on any pin does not conform with figure 5-4, troubleshoot card A2 pin K, J or T respectively using table 5-4.
3		Input signal defective for bit 2 or 5.	Send the letter R and observe pins V and K for conformance with figures 5-4. If data on either pin does not conform with figure 5-4, troubleshoot card A2 pins N or S respectively using table 5-4.

Table 5-5. Parallel Shift-Register Card A3, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
4		Flip-flop Z2 defective.	Send the letter Y and observe pins 16 and X for conformance with timing chart figure 5-4. If not in conformance, replace Z2.
5		Flip-flop Z3 defective.	Send the letter R and observe pins L and B for conformance with timing chart figure 5-4. If not in conformance, replace Z3.
6		Flip-flop Z4 defective.	Send the letter Y and observe pins H and J for conformance with timing chart figure 5-4. If not in conformance, replace Z4.
7		Flip-flop Z5 defective.	Send the letter R and observe pins 10 and C for conformance with timing chart figure 5-4. If not in conformance, replace Z5.
8		Flip-flop Z6 defective.	Send the letter Y and observe pins 15 and 7 for conformance with timing chart figure 5-4. If not in conformance, replace Z6.
9	No data, or incorrect data on pin 8; data on pins 14, L, H and 10 correct as the letter V is being sent.	Z9 defective.	Replace AND gate Z9.
10	Incorrect data on pins 17 and 18.	Z9 or Z11 defective.	Send the letter E and observe data on test point 1 for conformance with timing chart figure 5-4. If data conforms, replace AND gate Z11. If data does not conform, replace AND gate Z9.
11	Incorrect data during P interval on pins 8 and 14 as the letters Y and P are being sent.	Z11 defective.	Replace AND gate Z11.
12	As the letters Y and P are being sent: incorrect signal on pin S during Y interval and incorrect signal on pin P during P interval.	Z7 defective	Replace AND gate Z7.
13	As the letters Y, CR, blank and E are being sent: No data on pin 19 during CR interval; No data on pin 18 during blank interval; No data on pin 17 during E interval; Correct data on pin 14 and test point 1.	Z11 defective.	Replace AND gate Z11.

Table 5-5. Parallel Shift-Register Card A3, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
14	No data on pin P as the address is being sent.	Z1 or Z10 defective.	Observe data on test point 2 for conformance with timing chart figure 5-4 as the address is being sent. If data conforms, replace AND gate Z10. If data does not conform, replace flip-flip Z1.
15	No data on pin S; data on pin P.	Z10 defective.	Verify signals on pins B, J, C and 7 are in conformance with timing chart figure 5-4 as letter V is being sent. (Repeat sending V as required for remainder of step). If signals conform, replace AND gate Z7 and repeat step 15. If signal on pin S is still incorrect, replace AND gate Z10. If a signal on pin B, J, C or 7 is not in conformance with figure 5-4, verify its corresponding signal on pin V, F, K or 21 is in accordance with figure 5-4. If corresponding signal is correct, replace corresponding flip-flop for defective signal. If corresponding signal on pin V, F, K, or 21 is not correct, troubleshoot card A2 pin N, J, S or T respectively.
16	No data on pin R during S interval as letters Y, CR and S are being sent.	Z10 defective or incorrect input on pin N.	Observe pin N and pin 16 for data conformance with timing chart figure 5-5 during S interval as letters Y, CR and S are being sent. If data conforms, replace AND gate Z10. If data does not conform, troubleshoot output of pin T on card A6 in accordance with table 5-7.
17	No data on pins E or 3.	Z8 defective or input on pins 2 and 5 are missing.	Observe pins 2 and 5 for data conformation with timing chart figure 5-4 as letters Y and R are being sent. If data conforms, replace flip-flop Z8. If data does not conform, troubleshoot card A2 pins M and R in accordance with table 5-4.

TABLE 5-6. GATING CIRCUIT CARD A4, TROUBLESHOOTING

Step	Trouble	Probable Cause	Remedy
1	Output signal to decoder missing.	Start tune signal from A4 missing.	Address each decoder and perform step 4 and step 12, 20, 28, 36 or 44.

Table 5-6. Gating Circuit Card A4, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
2	No output on pin Y during E interval as letters Y, CR, Y, R and E are being sent.	Z1, Z2, Z3, Z4, Z5, Z7 or CR6 defective.	Perform steps 4 and 52, 53 and 54 as required.
3	Readback select out signal missing on pin 2, 3, 5, H or J as each decoder is addressed.	Z1, Z2, Z3, Z4, Z5, CR1, CR2, CR3, CR4 or CR 5 defective.	Perform steps 4, 55 and 56 as required.
4	No output signals on pins B, C, 6, 7 and 12 (after requesting that each decoder be addressed).	Z6 or Z7 defective, or signal on pin K, W, X, S or 11 in error.	Insert extender card between card A4 and its socket XA4. Perform steps 5, 6, 7, 8, 9, 10.
5		Wrong signal on pin K.	Verify signal on pin K conforms with timing chart Figure 5-7 as the letter E is being sent. If signal does not conform, troubleshoot card A6, pin S per table 5-6.
6		Wrong signal on pin W.	Verify signal on pin W conforms with timing chart figure 5-7 as the address is being sent. If signal does not conform, troubleshoot card A3, pin P per table 5-5.
7		Z7 defective.	Observe test point 24 for conformance with timing chart figure 5-7 as the address is being sent. If not present, replace AND gate Z7.
8		Z6 defective.	Observe test point 21 for same signal observed on test point 24 as the address is being sent. If observed signal is not the same, replace inverter Z6.
9		Wrong signal on pin X.	Verify signal on pin X conforms with timing chart figure 5-7 as the address is being sent. If signal does not conform, troubleshoot card A3, pin 19 per table 5-5.
10		Wrong signal on pin S.	Verify signal on pin S conforms timing chart figure 5-7 during E interval when address and E are sent. If signal does not conform, troubleshoot card A6, pin R per table 5-7.
11		Wrong voltage on pin 11.	Observe -12 VDC on pin 11. If signal is not -12 VDC, troubleshoot power supply card A10, pin 12 per troubleshooting table 5-9.

Table 5-6. Gating Circuit Card A4, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
12	No signal on pin 12 during E interval as address and E are being sent to equipment 1.	Wrong signal on pin P, T or U; Z1, Z6, Z10, CR7 or CR8 defective.	
13		Wrong signal on pin P.	Verify signal on pin P conforms with timing chart figure 5-7 as letters Y and R are being sent. If signal does not conform, troubleshoot card A3, pin 10 per table 5-5.
14		Wrong signal on pin T.	Verify signal on pin T conforms with timing chart figure 5-7 as letters Y and R are being sent. If signal does not conform, troubleshoot card A3, pin B per table 5-5.
15		Wrong signal on pin U.	Verify signal on pin U conforms with timing chart figure 5-7 as letters Y and R are being sent. If signal does not conform, troubleshoot card A3, pin J per table 5-5.
16		Z10 defective.	Verify signal on test point 16 conforms with timing chart figure 5-7 as address is being sent. If not, replace AND gate Z10.
17		Z1 defective.	Observe that signal on test point 9 assumes the '1' state when a '1' is applied to test point 16. If not, replace flip-flop Z1.
18		CR7 or CR8 defective.	Observe test point 5 for presence of a '1' when test point 9 is in '1' state and a '0' when test point 9 is '0'. If observation not verified, replace diode CR8 unless test point 5 is in '0' state when test point 9 is '1'. If this occurs, replace diode CR7.
19		Z6 defective.	If output on pin 12 is still incorrect when address is being sent to equipment 1, replace inverter Z6.
20	No signal on pin B during E interval when address and E are being sent to equipment 2.	Wrong signal on pin P, R or U; Z2, Z8, Z9 or Z10 defective.	
21		Wrong signal on pin P.	Perform step 13.
22		Wrong signal on pin U.	Perform step 15.

Table 5-6. Gating Circuit Card A4, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
23		Wrong signal on pin R.	Verify signal on pin R conforms with timing chart figure 5-7 as address is being spent. If signal does not conform, troubleshoot card A3, pin L per table 5-5.
24		Z10 defective.	Verify signal on test point 17 conforms with timing chart figure 5-7 as address is being spent. If not, replace AND gate Z10.
25		Z2 defective.	Observe that signal on test point 12 assumes the '1' state when a '1' is applied to test point 17. If not, replace flip-flop Z2.
26		Z9 defective.	Observe test point 2 for presence of a '1' when test point 12 is in '1' state and a '0' when test point 12 is '0'. If observation not verified replace AND gate Z9.
27		Z8 defective.	If output on pin B is still incorrect when address and E are being sent to equipment 2, replace inverter Z8.
28	No signal on pin 7 during E interval when address and E are being sent to equipment 3.	Wrong signal on pin R, M or N; Z3, Z8, Z9 or Z10 defective.	
29		Wrong signal on pin R.	Perform step 13.
30		Wrong signal on pin M.	Verify signal on pin M conforms with timing chart figure 5-7 as address is being sent. If signal does not conform, troubleshoot card A3, pin H per table 5-5.
31		Wrong signal on pin N.	Verify signal on pin N conforms with timing chart figure 5-7 as address is being sent. If signal does not conform, troubleshoot card A3, pin C per table 5-5.
32		Z10 defective.	Verify signal on test point 18 conforms with timing chart figure 5-7 as address is being sent. If not, replace AND gate Z10.
33		Z3 defective.	Observe that signal on test point 13 assumes the '1' state when a '1' is applied to test point 18. If not, replace flip-flop Z3.
34		Z9 defective.	Observe test point 3 for presence of a '1' when test point 13 is in '1' state and a '0' when test point 13 is '0'. If observation not verified replace AND gate Z9.

Table 5-6. Gating Circuit Card A4, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
35		Z8 defective.	If output on pin 7 is still incorrect during E interval when address and E are being sent to equipment 3, replace inverter Z8.
36	No signal on pin 6 during E interval when address and E are being sent to equipment 4.	Wrong signal on pin R, U or N; Z4, Z8, Z9 or Z11 defective.	
37		Wrong signal on pin R.	Perform step 13.
38		Wrong signal on pin U.	Perform step 15.
39		Wrong signal on pin N.	Perform step 31.
40		Z11 defective.	Verify signal on test point 10 conforms with timing chart figure 5-7 as address is being sent. If not, replace AND gate Z11.
41		Z4 defective.	Observe that signal on test point 8 assumes the '1' state when a '1' is applied to test point 10. If not, replace flip-flop Z4.
42		Z9 defective.	Observe test point 4 for presense of a '1' when test point 8 is in '1' state and a '0' when test point 8 is '0'. If observation not verified replace AND gate Z9.
43		Z8 defective.	If output on pin 6 is still incorrect during E interval when address and E are being sent to equipment 4, replace inverter Z8.
44	No signal on pin C during E interval when address and E are being sent to equipment 5.	Wrong signal on pin M, N or T; Z5, Z8, Z9 or Z11 defective.	
45		Wrong signal on pin M.	Perform step 30.
46		Wrong signal on pin N.	Perform step 31.
47		Wrong signal on pin T.	Perform step 14.
48		Z11 defective.	Verify signal on test point 11 conforms with timing chart figure 5-7 as address is being sent. If not, replace AND gate Z11.
49		Z5 defective.	Observe that signal on test point 7 assumes the '1' state when a '1' is applied to test point 11. If not, replace flip-flop Z5.

Table 5-6. Gating Circuit Card A4, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
50		Z9 defective.	Observe test point 1 for presence of a '1' when test point 7 is in '1' state and a '0' when test point 7 is '0'. If observation not verified, replace AND gate Z9.
51		Z8 defective.	If output on pin C is still incorrect during E interval when address and E are being sent to equipment 5.
52	No output on pin Y.	Z1, Z2, Z3, Z4, Z5, Z7 or CR6 defective.	Apply a ground to test points 10, 11, 16, 17 and 18. Observe pin Y for the presence of a '1'. If '1' is missing, observe test points 14, 19, 23, 6 and 22 for presence of the '1' state. If '1' is missing from a test point, replace its corresponding flip-flop (Z1, Z2, Z3, Z4, Z5 respectively).
53		CR6 defective.	If signal still a '0' on pin Y, replace diode CR6.
54		Z7 defective.	If signal on pin Y still a '0', replace AND gate Z7.
55	Readback select out signal missing on pin 2, 3, 5, H or J as corresponding equipments are addressed.	Z1, Z2, Z3, Z4, Z5 defective.	Verify status of flip-flops Z1, Z2, Z3, Z4 and Z5 by performing steps 17, 25, 33, 41 and 49 respectively.
56		CR1, CR2, CR3, CR4 or CR5 defective.	Repeat steps 17, 25, 33, 41 and 49 while observing pins 2, 3, 5, H and J respectively for a '1' state each time its associated test point (9, 12, 13, 8 or 7) respectively assumes the '1' state.

TABLE 5-7. SHIFT TIMING CARD A6, TROUBLESHOOTING

Step	Trouble	Probable Cause	Remedy
1	No output on pin C	Inverter Z4 defective or input from A11 missing.	Observe pin B for data as two different equipments are individually addressed. If data present, replace inverter Z4. If data not present, troubleshoot readback selector card A11, pin F in accordance with troubleshooting table 5-10.
2	No output or incorrect output, on pin K as a blank is being sent.	Inverter Z9 defective or input from A3 missing or incorrect.	Observe pin L for data in accordance with figure 5-4, pin 18 as a blank is sent. (Negative for duration of blank pulse.) If data in accord with figure, replace inverter Z9. If not in accord,

Table 5-7. Shift Timing Card A6, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
			troubleshoot parallel shift register card A3 in accordance with troubleshooting table 5-5.
3	No output on pin S.	Emitter follower Z10 defective.	Replace emitter follower Z10.
4	No output on pin S14 as the letter V is being sent.	Inverter Z9, emitter follower Z10 defective or input from card A3 missing.	Observe pin 6 for data in accordance with timing chart figure 5-4, pin 8 as V is being sent. If no data present or data not per timing chart, troubleshoot parallel shift-register card A3, pin 8 using table 5-5. If data is satisfactory, observe test point 10 for inverse of data on pin 6 as V is being sent. If data not correct, replace inverter Z9. If data is correct replace emitter follower Z10.
5	No output on pin E as address and E are being sent.	Z4 defective or no signal on pin D.	Observe signal on pin D for conformance with timing chart figure 5-5 (inverse of data shown for pin 2). If observed data conforms, replace inverter Z4. If observed data does not conform, troubleshoot gating circuit card A4 per table 5-6, pin Y.
6	No output on pin T; Output on pin E during letter Y interval as address, CR, and Y are sent.	Z6 defective.	Replace AND gate Z6.
7	No output on pins P and V as address and Y's and R's are sent.	Input from decoder in error, diode CR3 or CR4 defective or Z3 or Z2 defective.	Observe pin U for absence of a ground. If a ground is observed, decoder signal defective. Verify a negative voltage on test point 5. If negative voltage not present, replace diode CR3 or registor R7. Observe test point 2 for a '0' if '0' not present, replace inverter Z3; if '0' is present, observe test point 15 for approx. -4.5 VDC. If -4.5 VDC is not present, replace timing generator Z2; if -4.5 VDC is present, observe test point 8 for a '1'. If '1' is not present, replace inverter Z3. If still no signal, replace diode CR4.
8	No output on pin P; Output on pin V as address Y's and R's are sent.	Inverter Z3 defective.	Replace inverter Z3.
9	No output on pin T as address is sent and followed with a series of Y's.	Z6 or CR2 defective.	Observe test point 9 for data in conformance with timing chart figure 5-5, TP9. If data not correct, replace diode CR2. If data is correct, replace AND gate Z6.

Table 5-7. Shift Timing Card A6, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
10	No output on pins P, R, S and T as address and letter E are sent.	No input on pin 3, 19 or 21; Z8 or Z11 defective.	Verify signal on pin 3 is inverse of signal on test point 8 of card A2; if signal is incorrect, troubleshoot clock timing circuit card A2, pin R per table 5-4. Verify signal on pin 19 conforms to timing chart figure 5-4, pin 17. If data not per timing chart, troubleshoot card A3, pin 17 per table 5-5. If data on pin 19 is correct, verify data on pin 21 conforms to data for pin W on card A2 timing chart, figure 5-3. If data on pin 21 not per timing chart, troubleshoot card A2, pin W per troubleshooting table 5-4. Observe test point 14 on card A6 for data per timing chart figure 5-6, TP14. If data not per timing chart, replace AND gate Z11; if data is per timing chart, replace flip-flop Z8.
11	No data on pin R; Signal on TP9 as address and letter E are sent.	Z6 defective.	Replace AND gate Z6.
12	No data on pins R, T and V as address and letter E are sent.	No input on pin 6; Z9 or Z10 defective.	Observe signal on pin 6 for conformance with data as shown on timing chart figure 5-4, pin 8. If data does not conform, troubleshoot card A3-pin 8 using table 5-5; if data does conform, observe test point 10 for conformance with timing chart figure 5-5. If data conforms with figure 5-5, replace emitter follower Z10; if not, replace inverter Z9.
13	No data on pin V as address and a series of alternate Y's and R's are sent.	No input on pin J, W, X, or 7; or Z9, Z5, Z4, Z11, Z1, Z3 or Z7 defective.	Verify data on pins W and X in conformance with data shown on timing chart, figure 5-5. If data does not conform, troubleshoot clock timing circuit card A2, per table 5-4 (pins P and V). Verify data on pin 7 is in conformance with timing chart, figure 5-5. If data does not conform, troubleshoot parallel shift-register card A3 per table 5-5, pin S. Verify data on pin J in conformance with timing chart figure 5-5. If data does not conform, troubleshoot integrated shift-register card A7, pin E using table 5-8.
14		Z9 defective.	Observe signal on pin 8 for conformance with data on timing chart figure 5-5. If data does not conform, replace inverter Z9.

Table 5-7. Shift Timing Card A6, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
15		Z5, Z4, or Z1 defective.	Observe data on test points 4, 3 and 1 for conformance with data as shown on timing chart figure 5-5. If data at any test points does not conform, replace the integrated circuit which it samples.

TABLE 5-8. INTEGRATED SHIFT-REGISTER CARD A7, TROUBLESHOOTING

Step	Trouble	Probable Cause	Remedy
1	Bit information to decoder not as sent.	Component in card A7 defective or incorrect signal being fed to card A7.	Troubleshoot integrated shift-register card A7, shift timing circuit card A6, and/or parallel shift-register card A3.
2			Insert extender card between card A7 and its socket XA7.
3	No data transfer to decoder.	Memory shift pulse from card A6 missing or AND gate Z6 defective.	While observing pin 6, send address, and a series of Y's and R's to station being serviced (repeat as required) and verify input signal on pin 6 and test point 7 conforms to timing chart figure 5-6, pin V. If signal on pin 6 does not conform to timing chart, troubleshoot card A6, pin V, per table 5-7. If signal is in accord with timing chart on pin 6 and not per timing chart on test point 7, replace AND gate Z6.
4	No data on TP1, TP3, TP5 and TP14 as address Y's and R's are being sent.	Memory 'A' Input Gate Control signal from A6 defective.	Troubleshoot card A6, pin T per table 5-7.
5	No data on TP1, TP3, TP5 or TP14 as address, Y's and R's are being sent.	Card A3, or Z11 on card A7 defective.	Observe input signals on pin U and Y for presence of '1's and on pins X and W for presence of '0' as the address and a series of R's are sent. If signal on any pin is not correct, troubleshoot card A3, pin L, 10, H or 15 respectively, as required, per table 5-5. Observe input signals on pins U and Y for presence of '0's and on pins X and W for presence of '1's as address and a series of Y's are sent. If signal on any pin is not correct, troubleshoot card A3, pin L, 10, H or 15 respectively, as required, per table 5-5.

Table 5-8. Integrated Shift-Register Card A7, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
6		AND gate Z11 defective.	Observe during R interval presence of '1's on test points 1 and 5, and '0's on test points 3 and 14 when the address and letter R is sent. If any observed signal is in error, replace Z11. Observe during Y interval presence of '0's on test points 1 and 5, and '1's on test points 3 and 14 when the address and letter Y is sent. If any signal is in error, replace Z11.
7	No signal on pin E as letter E is being sent.	Card A6 defective.	Observe signal on pin 5 for conformance with table 5-8 as letter E is being sent. If signal does not conform, troubleshoot card A6 pin S using table 5-7.
8		Z6 defective.	Observe signal on TP8 for conformance with table 5-8 as letter E is being sent. If signal defective, replace Z6.
9		Z8 defective.	Observe signal on pin E for conformance with table 5-8 as letter E is being sent. If signal defective, replace Z8.
	Note: For the remaining steps in this table the RTMU must be connected to a decoder/equipment network which are being controlled by this RTMU. When instructed to send a program, the technician is to send a full program using table 4-1. Use test point 7 as scope sync for steps 11 through 18.		
10	'Bit 1 monitor' or 'Bit 1 (SGL & DUAL A1-5) signal missing or in error as address, a series of Y's and R's and an E are being sent.	Card A3 defective.	Observe pin 2 for presence of signal per figure 5-8 as address, a series of Y's and R's and an E are being sent. If signal defective, troubleshoot card A3 pin R using table 5-5.
11		Z1 defective	Observe pin 3 of Z8 for change of state as full program is sent. If no change of state observed, replace Z1.
12		Z8 defective.	Observe test point 9 and pin D for a change of state as full program is sent. If no change of state observed, replace Z8.
13		Z6 defective.	Observe test point 8 for change of state as full program is sent. If no change of state observed, replace Z6.

Table 5-8. Integrated Shift-Register Card A7, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
14		Z8 defective.	Observe pin E for change of state as a full program is sent. If no change of state, replace Z8.
15	No instructions to equipment.	Card A3 defective.	Observe pin V for signal per table 5-8. If signal defective, troubleshoot card A3 using table 5-5.
16	Instructions to equipment not as sent by remote operator.	Z2, Z3, Z4, or Z5 defective.	Observe test points 2, 4, 6 and 15 for change of state as a full program is sent. If no change of state observed on any of these test points; perform troubleshooting from step 3 as required. If change of state not observed on a test point, replace its corresponding shift register.
17		Z7 defective.	Observe test points 10, 11, 12 and 13 for a change of state as a full program is sent. If change of state missing on any of these test points, replace Z7.
18		Z9 defective.	Observe pins 9, 10, 11 and J for a change of state as a full program is sent. If a change of state is not observed on any pin, replace Z9.

TABLE 5-9. POWER SUPPLY CARD A10, TROUBLESHOOTING

Step	Trouble	Probable Cause	Remedy
1	No -12 vdc on any card.	Chassis mounted rectifier CR2, capacitor C3, transormer T1 or transistor Q1 defective.	Insert extender card between card A10 and its socket XA10.
2		Transformer defective.	Observe POWER indicator. If not lit, measure voltage between transformer terminals 11 and 12. If no voltage is measured, replace transformer T1.
3		Rectifier CR2 or capacitor C3 defective.	Observe voltage between pins H (-) and N (+). If no voltage is measured, verify status of chassis mounted capacitor C3. If defective, replace C3 and rectifier CR2. If capacitor is not defective, replace rectifier CR2.
4		Chassis mounted transistor Q1, card mounted transistor Q3 or voltage regulator Z2 defective.	Sequentially replace the following components until -12 vdc is observed between pins L and A: Transistor Q1, Q3 voltage regulator Z2. If voltage is still not observed, inspect other -12 volt power supply components and replace any which are found defective.

Table 5-9. Power Supply Card A10, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
5	No +12 vdc on any card.	Card A10 defective or input power from transformer T1 missing.	Insert extender card between card A10 and its socket XA10.
6		Transformer T1 defective.	Observe pins 16 and 17 for 18 VAC. if not voltage observed, replace transformer T1.
7		Rectifier CR2 or resistor R29 defective.	Observe pins V (+) and 22 (-) for a dc voltage. If dc voltage is not observed, verify resistor R29 is approximately 1 ohm. If R29 is not 1 ohm, replace it. If R29 is 1 ohm, replace rectifier CR2.
8		Transistor Q4, Q5 or voltage regulator Z3 defective.	Sequentially replace the following components until +12 vdc is observed between pins X (+) and 22 (-): Transistor Q4, Q5; voltage regulator Z3. If voltage is still not observed, inspect other +12 volt power supply components and replace any which are defective.
9	No -27 vdc on any card.	Card A10 defective or input power from transformer T1 missing.	Insert extender card between card A10 and its socket XA10.
10		Transformer T1 defective.	Observe pins 6 and 7 for 27 VAC. If no voltage observed, replace transformer T1.
11		Rectifier CR1 or resistor R21 defective.	Observe pins D (+) and 3 (-) for a dc voltage. If dc voltage is not observed, verify resistor R21 is approximately 1 ohm. If R21 is not 1 ohm, replace it. If it measures 1 ohm, replace rectifier CR1.
12		Transistor Q2, Q1 or voltage regulator Z1 defective.	Sequentially replace the following components until -27 vdc is observed between pins F (-) and 1 (+): Transistor Q2, Q1; voltage regulator Z1. If voltage is still not observed, inspect other -27 volt power supply components and replace any which are defective.

TABLE 5-10. READBACK SELECTOR CARD A11, TROUBLESHOOTING

Step	Trouble	Probable Cause	Remedy
1	Stepping switch does not operate.	Input signals are missing, card A11 or card A6 is defective.	Insert an extender card between card A11 and its socket XA11. Proceed to step 2, 3, 4 or 5 as required.

Table 5-10. Readback Selector Card A11, Troubleshooting (Continued)

Step	Trouble	Probable Cause	Remedy
2		Input signal missing.	Address each of the five decoders while observing the corresponding pins on the extender card. Repeat the address as required. Note: pin numbers are equivalent to decoder numbers. If signal is missing on any pin number, troubleshooting corresponding source pin on card A4 using troubleshooting table 5-6.
3		Card A6 is defective.	Observe pin W for dc voltage while addressing each decoder. If no voltage is observed, troubleshoot card A6 per table 5-7.
4		Card A11 defective.	With an ohmmeter, verify continuity of inductor, L1; status of diode, CR2; resistor R1 and capacitor C1. If a component is defective, replace it.
5		Stepping switch or SCR defective.	Measure voltage across stepping switch coil as SCR is activated by a signal. If voltage is zero, replace SCR. If a voltage exists, replace the stepping switch.

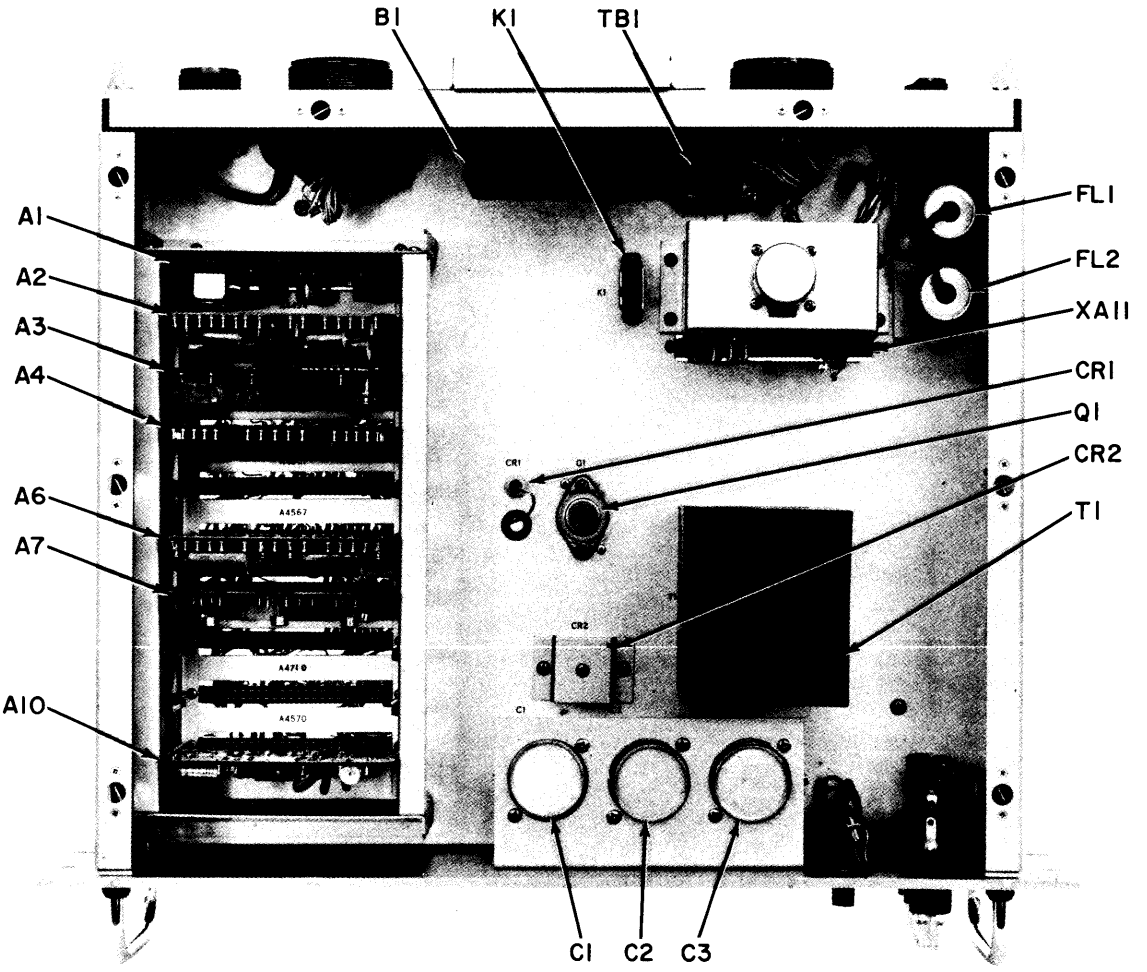
Prior to troubleshooting a card, its input voltages should be verified as listed in Section 2, paragraph 2-5c. If any voltage is in error, troubleshoot card A10 using table 5-9.

Because of the complex interaction of card circuits it is important that cards are not removed during measurement of their inputs and outputs as outlined in table 5-2. An extender card is to be inserted between the card being investigated and its socket in order to maintain loop circuitries. All inputs and outputs of a card should be verified, if possible, before removal of extender card. It is assumed that when checking outputs, should the reason for the absence of any output be found attributable to the absence of an input signal, the technician will next check the card suppling the missing input. The technician is to set the POWER switch "OFF" prior to removing any card. Likewise, unless instructed to the contrary, he is to set the POWER switch to "ON" after card, or extender card + card, are reinserted. The technician is also to remove the extender card at completion of testing unless instructed otherwise. Refer to Functional Servicing Block Diagram, figure 4-1. Figures 5-1 and 5-2 show respective top and bottom views of the equipment.

When instructed to initiate or send a letter, message or instruction, the technician will connect a TTY keyboard as shown in figure 2-4 and utilize the keyboard for signal generation.

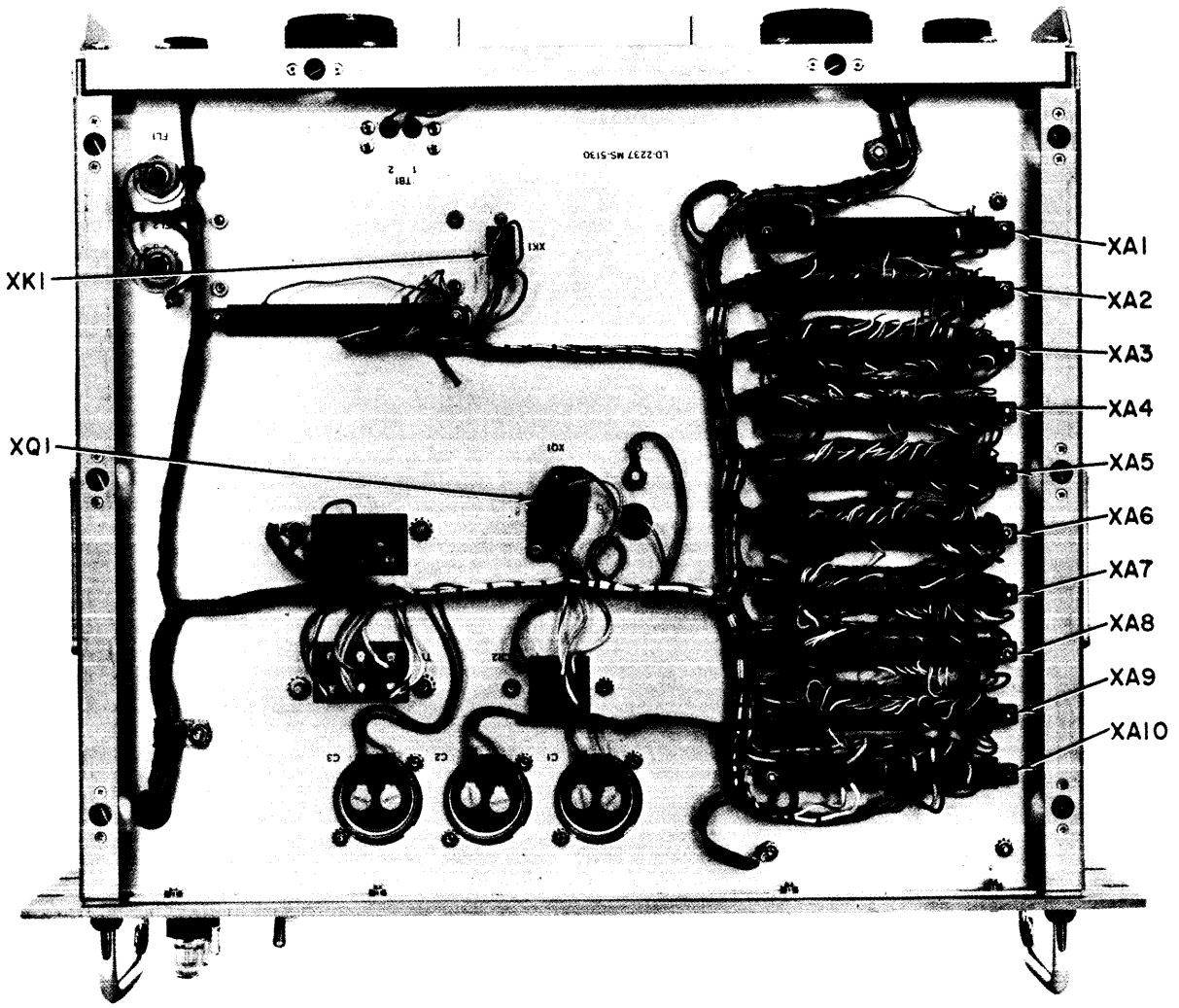
USAGE OF TIMING CHARTS - Timing charts (figures 5-3 through 5-8) are categorized by individual printed circuit boards involving binary logic and subdivided further into the phases and modes of these boards. Each line represents a test point time variance between two voltage values and all lines are plotted against a common time base for comparison. Test points are arranged from top to bottom in normal order of checking (from input to output) of a functional section, or subdivision thereof.

Using time bases A and B of the oscilloscope, check test points in pairs (the test point and the one directly below it on the chart) at coinciding pulse edges (voltage changes). This comparison check will reveal, by reference to the P/C board logic/schematic in section 7, the logic network/component to be replaced. To make a measurement, set the oscilloscope for an external triggering mode, with a negative triggering slope and level for a negative-going change and a positive triggering slope and level for a positive-going change. The exact shape of the pulse edge is not an important factor in troubleshooting the binary logic sections. Very often, different attenuator lines into the oscilloscope will produce pulse shape distortions that are not present in the



69 4.22-4

Figure 5-1. Major Component Location Diagram, Top View



69 4.22-5

Figure 5-2. Major Component Location Diagram, Bottom View

equipment being tested. The critical fact is whether or not the expected voltage changes occur in the polarities and coincidences as indicated on a common time base.

Note

THE SIGNAL SHOULD ALWAYS BE PRECEDED WITH THE FIRST TWO SELECTION CODES FOR THE RTMU/EQUIPMENT BEING ADDRESSED.

Equipment address, for the equipment being serviced, can be determined by reference to the "Equipment Selection Jumpter Guide" table on figure 7-4. Since the RTMU has a limited memory storage, it is imperative that each troubleshooting step which utilizes the TTY keyboard be preceded by the correct equipment address. Do not activate keys on the keyboard in excess of 32 times without reentering the equipment address.

5-3. ADJUSTMENTS

For adjustments of the RTMU-41A, refer to Section 2, paragraph 2-5d.

5-4. REPAIR OF PRINTED CIRCUITRY

a. Introduction - Repair of the chassis-mounted circuitry follows standard laboratory procedures. Repair of printed circuit cards and card receptacle wiring, however, requires the special tools and techniques as outlined here. Section 6, Parts List, lists all replaceable parts and their circuit symbol numbers. These symbol numbers are shown on the figures provided in Section 7.

Note

Replacement of parts on the printed circuit boards requires the special tools described in paragraph 5-4b through d.

b. Replacement of Parts - When replacing a part on a board, it is necessary to remove the old part from the board by melting the solder on all component pins. Soldering the new part to the board is done pin-by-pin with conventional methods.

c. Check Printed Circuit Conductors - Breaks in the conducting strip (foil) on a printed circuit board can cause permanent or intermittent trouble. In many instances, these breaks will be so small that they cannot be detected by the naked eye. These invisible cracks (breaks) can be located only with the aid of a powerful magnifying glass.

To check out and locate trouble in the conducting strips of a printed circuit board, set up a multimeter (one which does not use a current in excess of 1 ma) for making point-to-point resistance tests, using needle probes. Insert one point into the conducting strip, close to the end of terminal, and place the other probe on the terminal or opposite end of the conducting strip. The multimeter should indicate continuity. If the multimeter indicates an open circuit, drap the probe along the strip (or if the conducting strip is coated, puncture the coating at intervals) until the multimeter indicates continuity. Mark this area; then use a magnifying glass to locate the fault in the conductor.

CAUTION

Before using an ohmmeter for testing a circuit containing transistors or other voltage-sensitive semi-conductors, check the current it passes under test on all ranges. DO NOT use a range that passes more than 1 ma.

d. Repair Of Printed Conductors - If the break in the conductor strip is small, lightly scrape away any coating coverting the area of conducting strip to be repaired. Clean the area with a firm-bristled brush and approved solvent. Then repair the cracked or broken area of the conducting strip by flowing solder over the break. Considerable care must be exercised to keep the solder from flowing onto an adjacent strip.

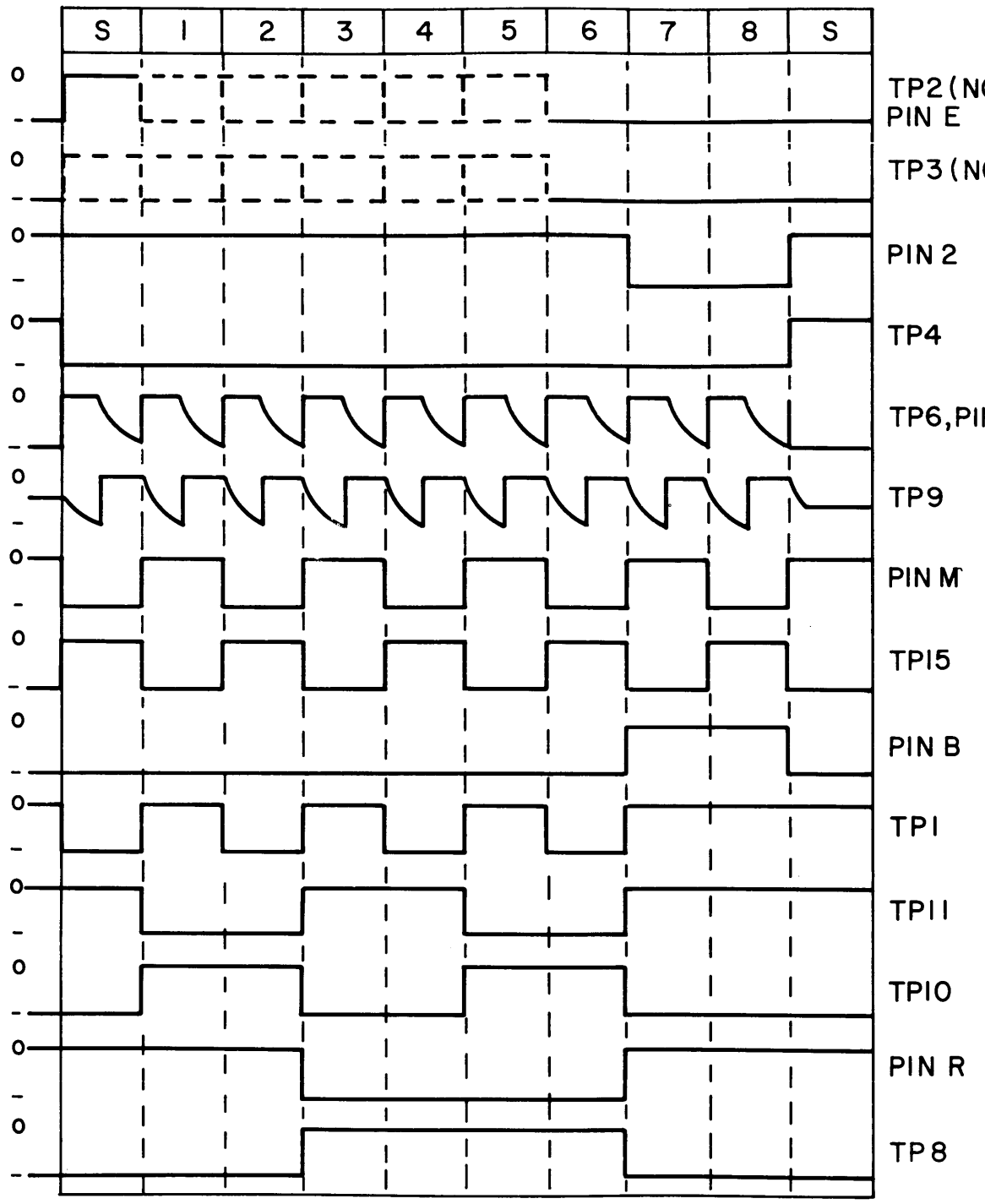
If a strip is burned out, or fused, cut and remove the damaged strip. Connect a length of insulated wire across the breach or from solder point to solder point.

After the repairs are completed, clean the repaired area with a stiff brush and solvent. Allow the board to dry thoroughly, and then coat the repaired area with an epoxy resin or similar compound. This coating not only will protect the repaired area, but will help to strengthen it.

CAUTION

After repairs, check the board for solder drippings; they may cause shorts.

Frequently, a low-resistance leakage path will be created by moisture and/or dirt that has carbonized onto the phenolic board. This leakage can be detected by measuring the suspected circuit with a multimeter. To overcome this condition, thoroughly clean the carbonized area with solvent and a stiff brush. If this does not remove it, use a scraping tool (spade end of a solder-air tool or its equivalent) to remove the carbon, or drill a hole through the leakage path to break the continuity of the leakage. When the drilling method is used, be careful not to drill into a part mounted on the other side.



Note 1. Input Code for letter R is 01010
Input Code for letter Y is 10101
where a '0' is zero volts and
a '1' is a negative voltage.

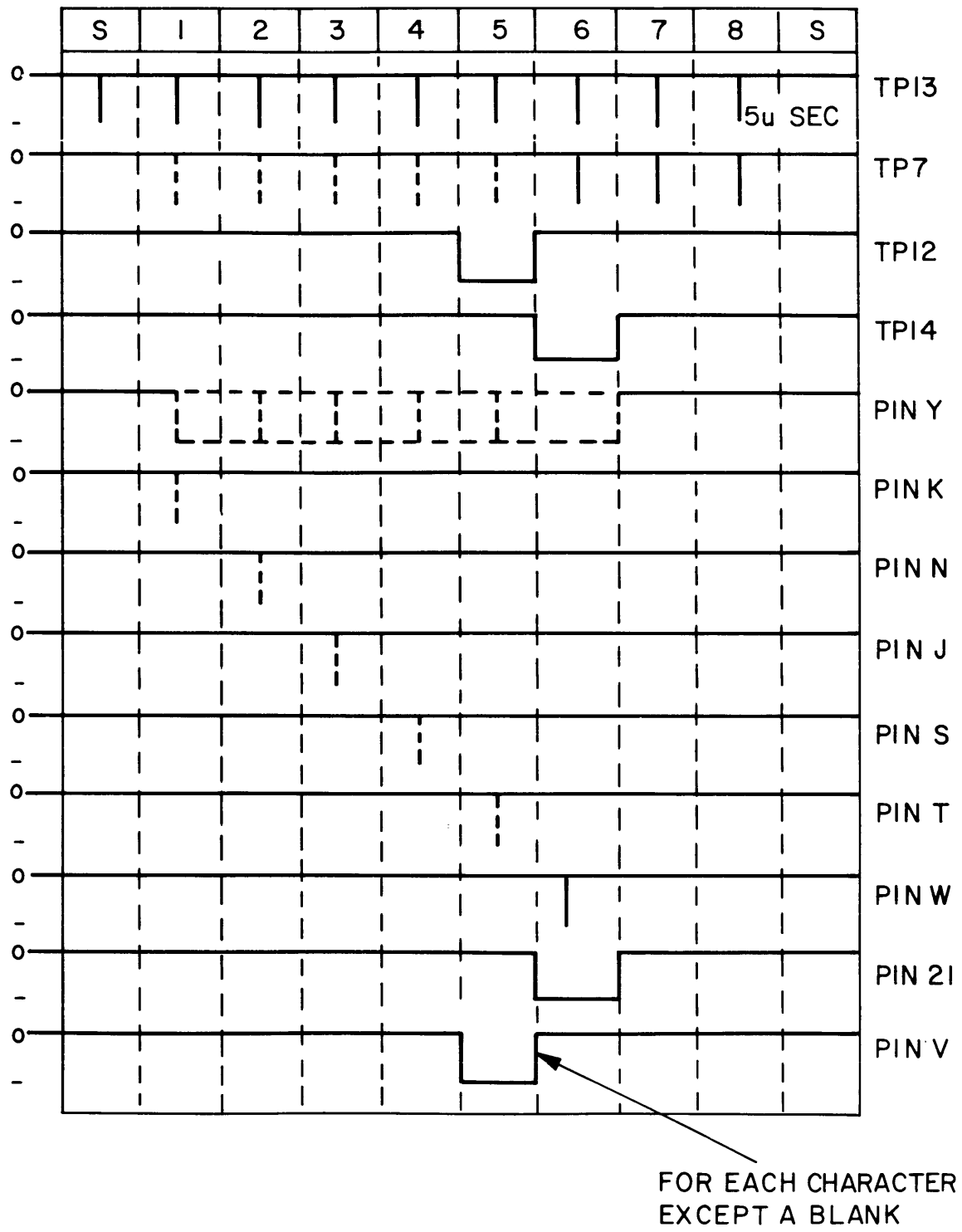
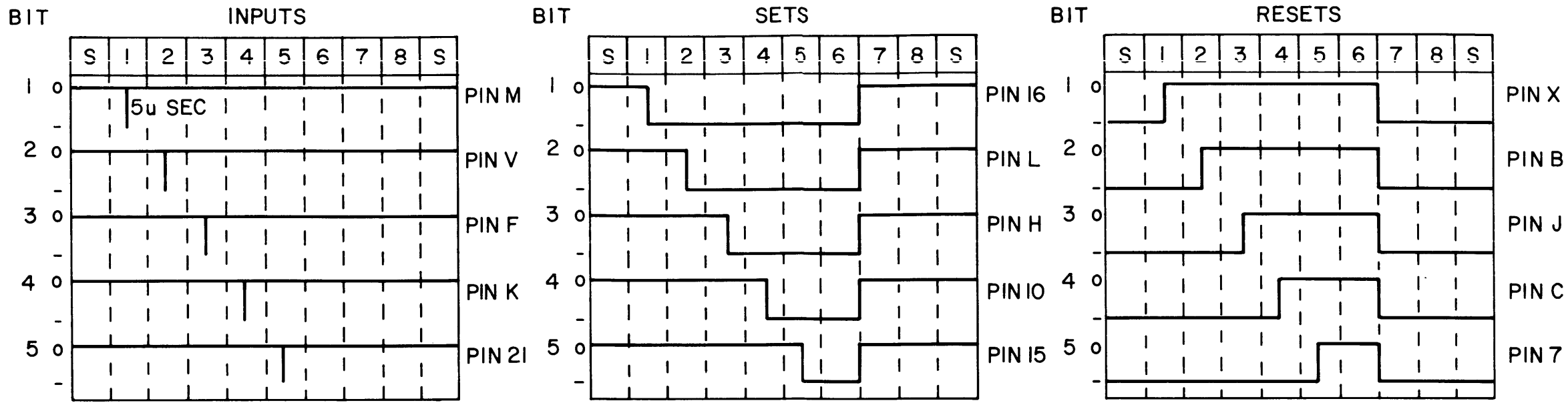


Figure 5-3. Timing Chart, Clock Timing Circuit Card, A2



NOTE: The above waveforms are present only for characters containing those bits. When a bit is not present in a character code, the signals will remain at their static levels for the duration of that character. (Static levels: BIT INPUTS - 0 VDC, BIT SETS - 0 VDC, BIT RESETS - -10 VDC).

FF Z8 CLOCK STOP

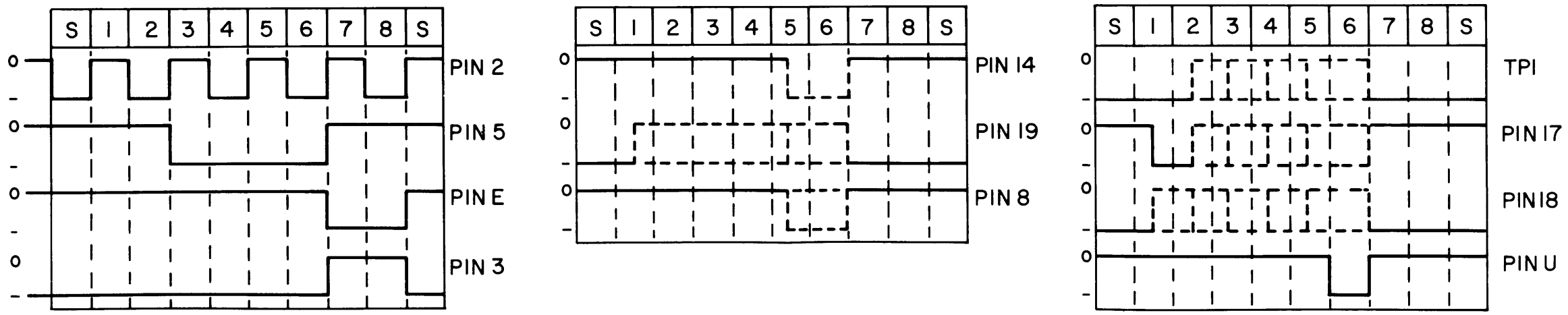


Figure 5-4. Timing Chart, Parallel Shift-Register Card, A3 (Sheet 1 of 2)

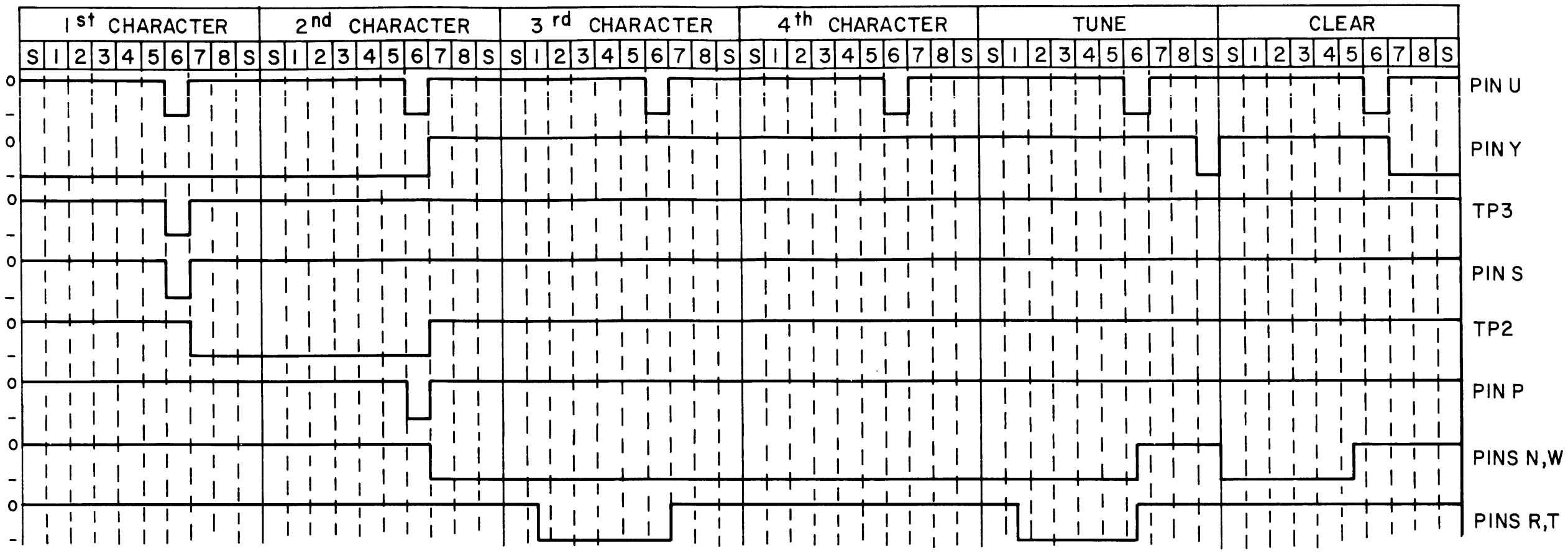
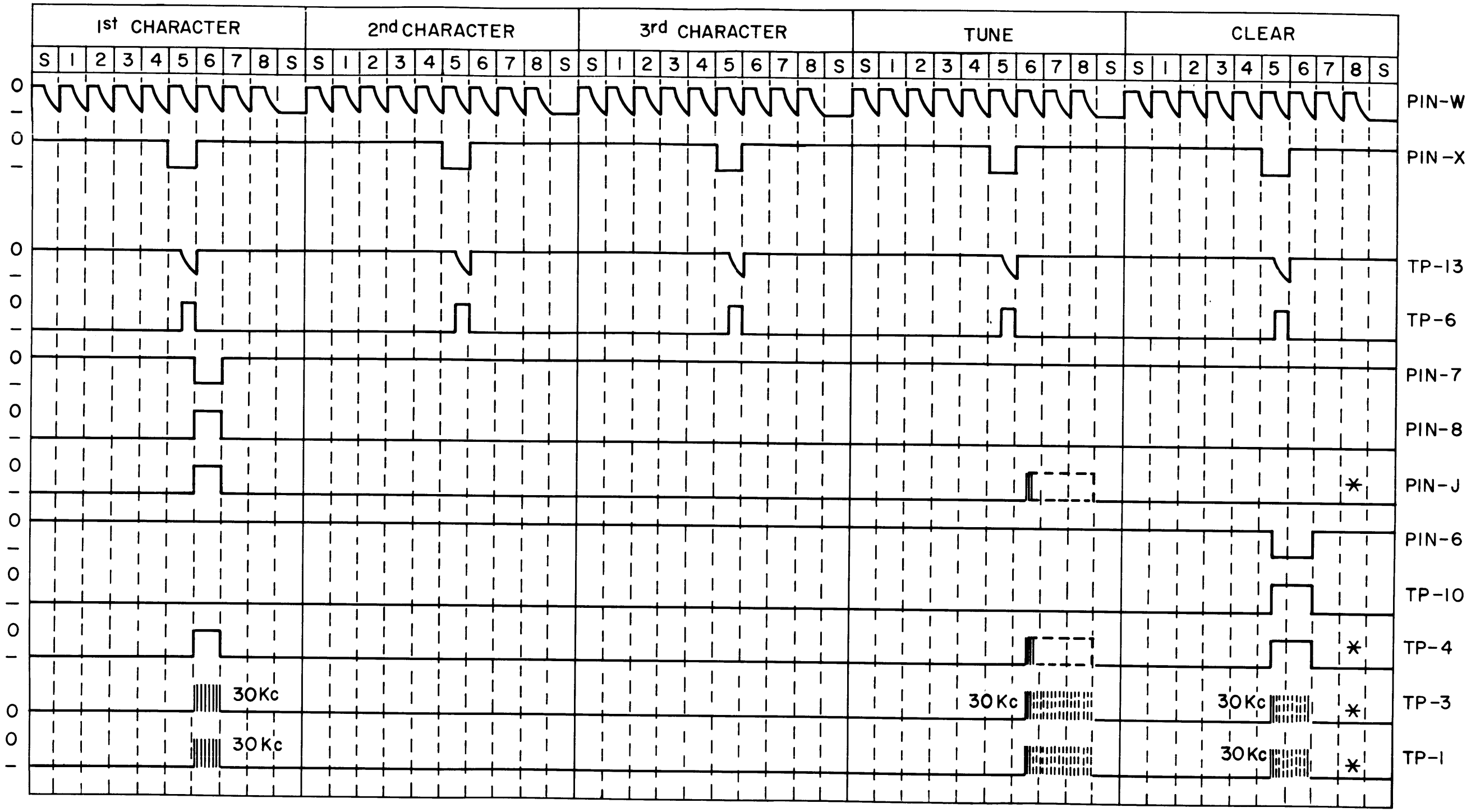


Figure 5-4. Timing Chart, Parallel Shift-Register Card, A3 (Sheet 2 of 2)



*NOTE: The waveforms shown in solid lines for the TUNE character are generated by the action of an RTTD when there is a program. With no program, the waveforms shown in broken lines will be present.

Figure 5-5. Timing Chart, Shift Timing Circuit Card, A6 (Sheet 1 of 2)

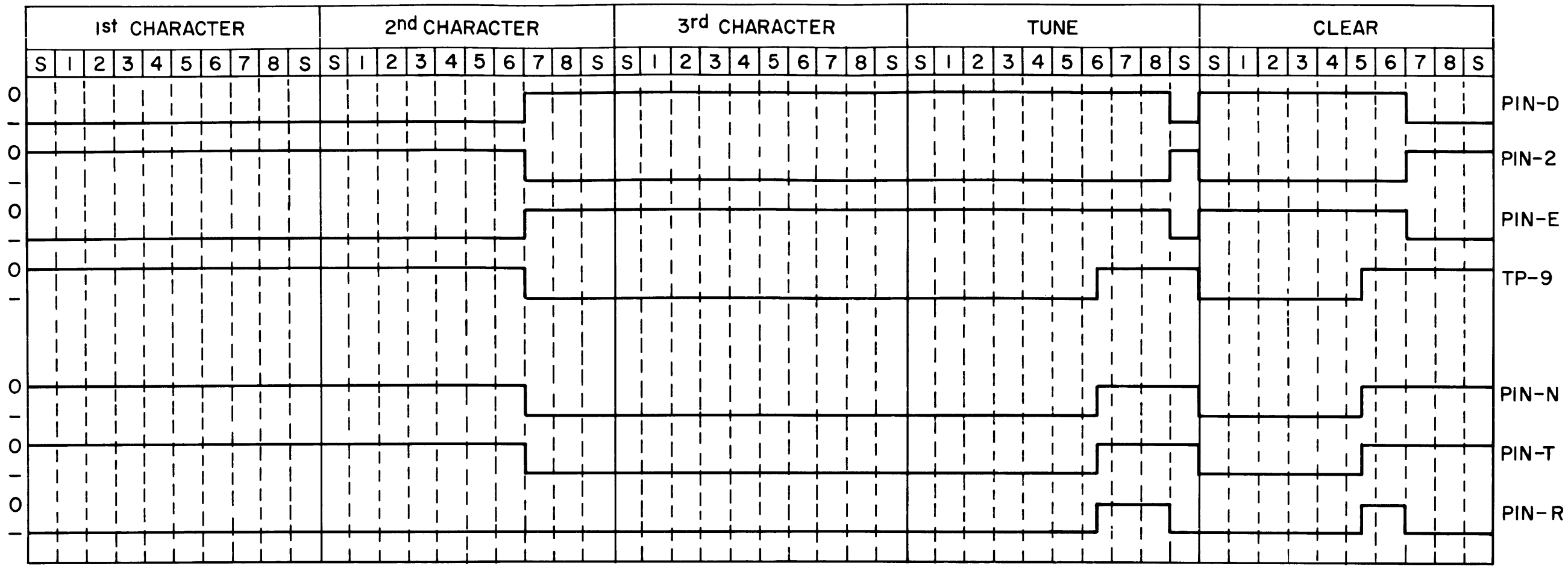
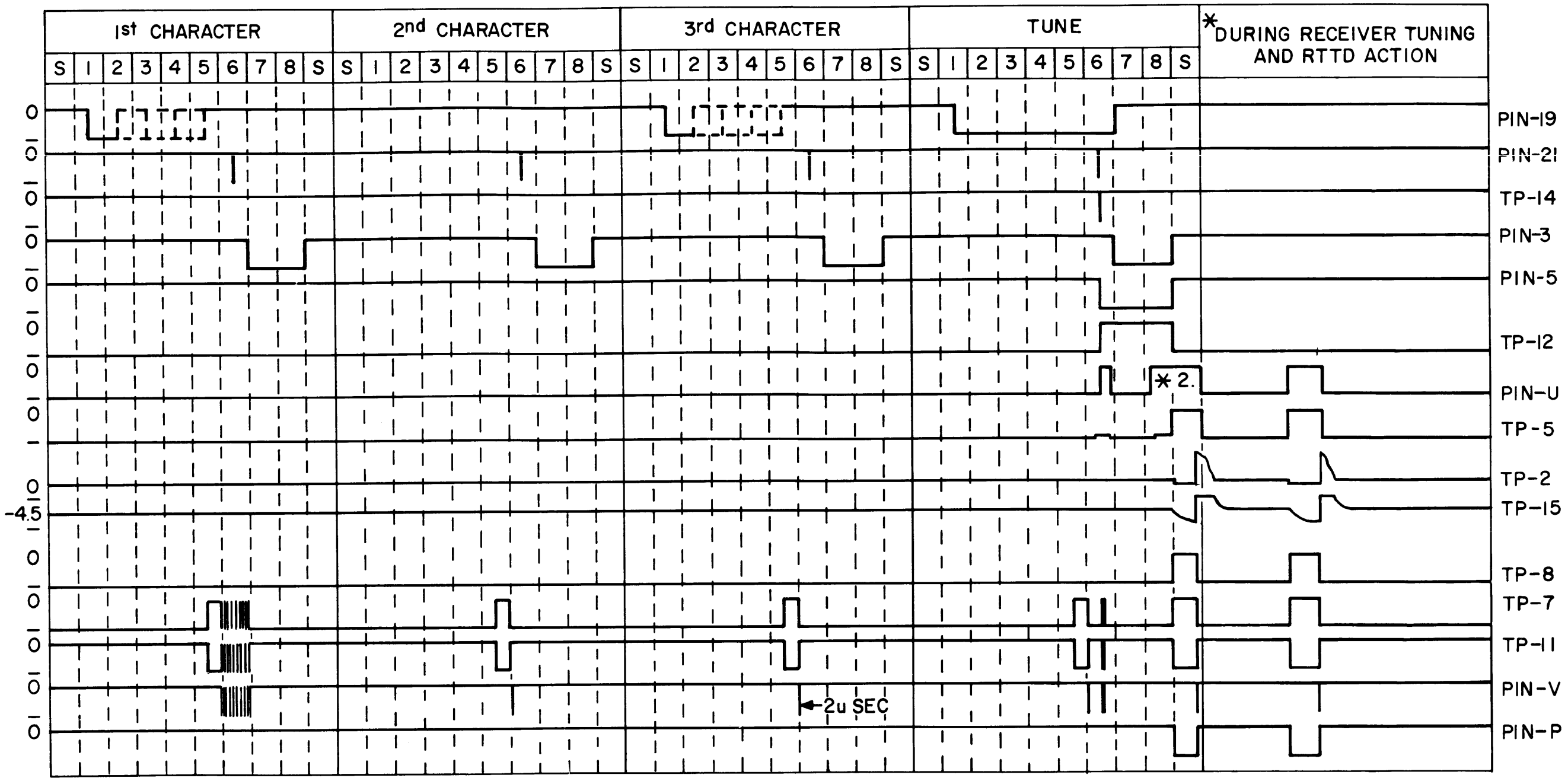


Figure 5-5. Timing Chart, Shift Timing Circuit Card, A6 (Sheet 2 of 2)

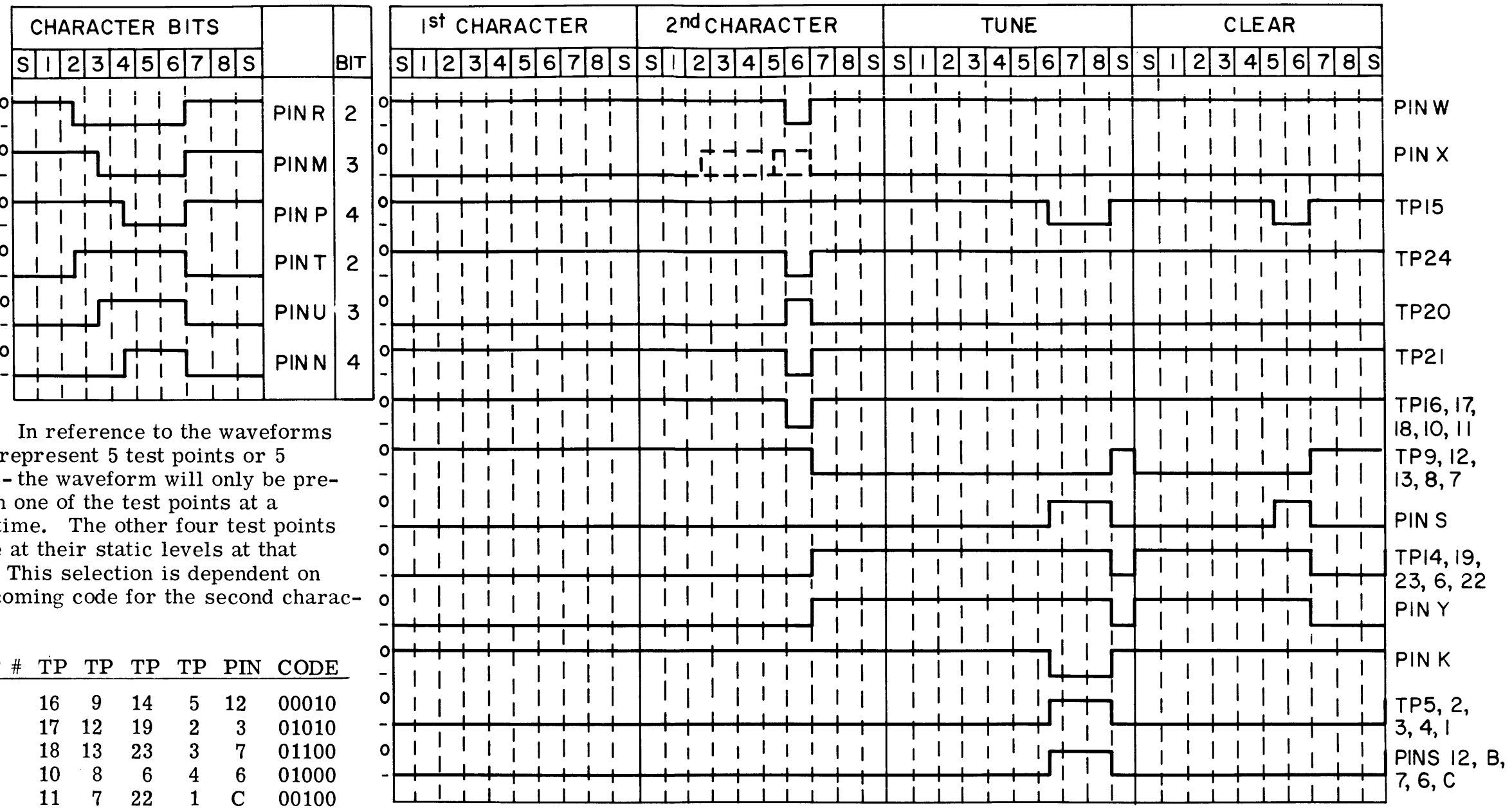


*NOTE: 1. The waveforms shown "During Equipment Tuning and RTTD Action" are representative of a particular program. The program used to generate these waveforms is, "changing the 10 mcs selector switch on the HFSR from position 0 to position 2". Any program will cause a series of positive signals at pin U (from the RTTD) as the RTTD and Receiver ledexes position. These incoming signals at pin U will cause the RTMU to generate shift pulses at pin V in accordance with the program (similar to those shown for this particular program).

2. The waveform on pin U generated during Bit 8 of the Tune character is present only when the 10 mcs selector switch is a part of the program.

Figure 5-6. Timing Chart, Shift Timing Circuit Card, A6

NOTE: The waveforms below are present only for characters containing those bits.



NOTE: In reference to the waveforms which represent 5 test points or 5 pins, -- the waveform will only be present on one of the test points at a given time. The other four test points will be at their static levels at that time. This selection is dependent on the incoming code for the second character.

REC #	TP	TP	TP	TP	PIN	CODE
1	16	9	14	5	12	00010
2	17	12	19	2	3	01010
3	18	13	23	3	7	01100
4	10	8	6	4	6	01000
5	11	7	22	1	C	00100

Figure 5-7. Timing Chart, Gating Circuit Card, A4

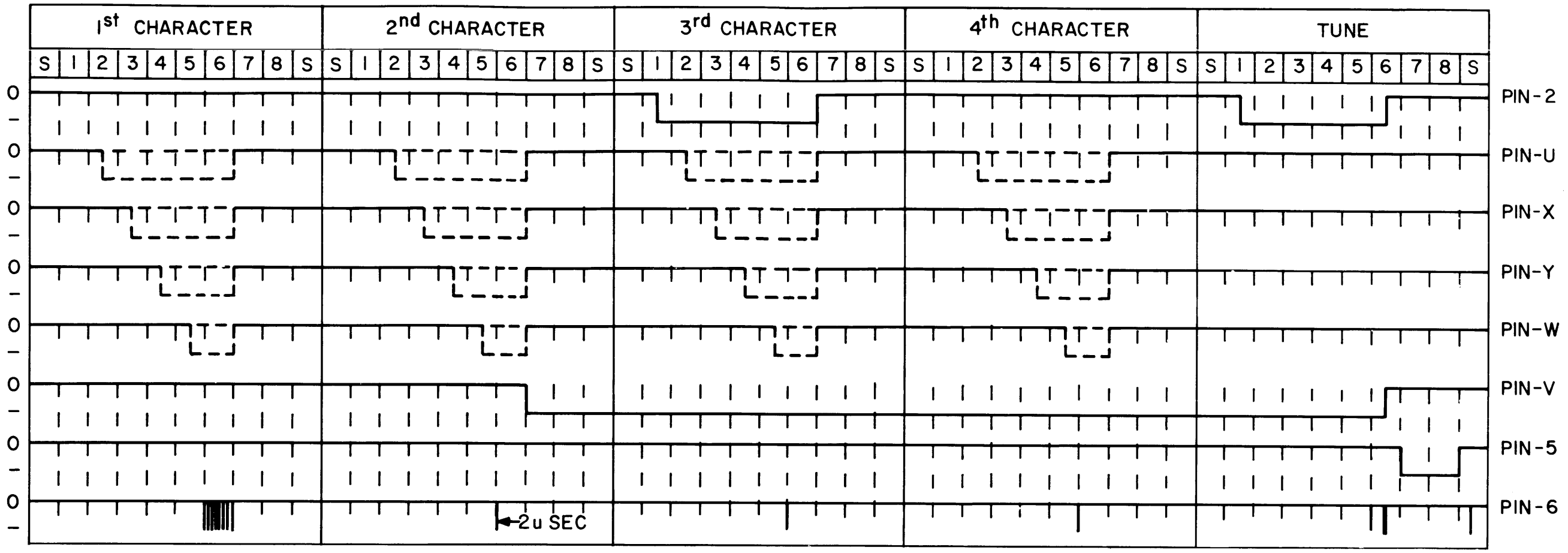
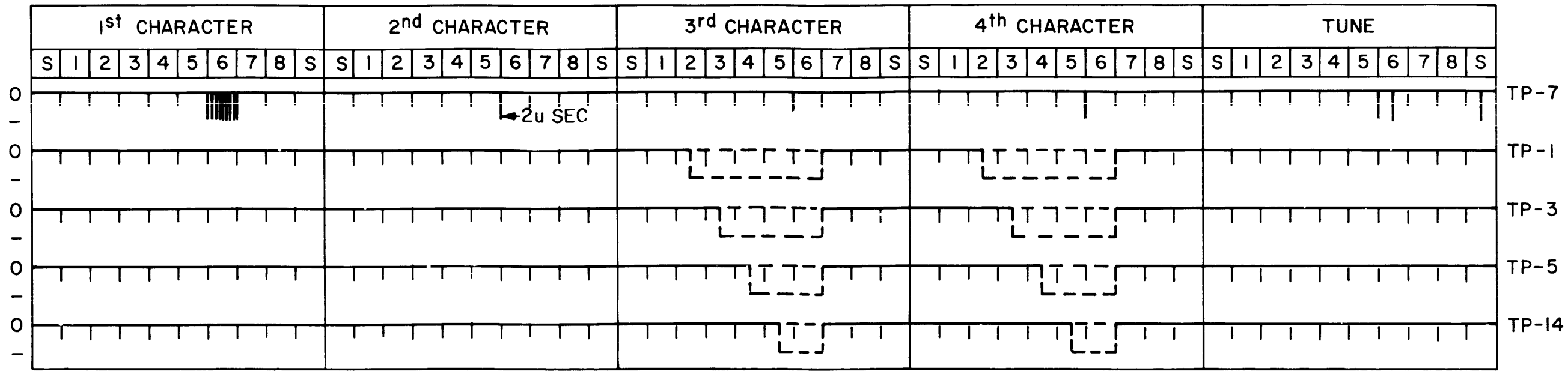
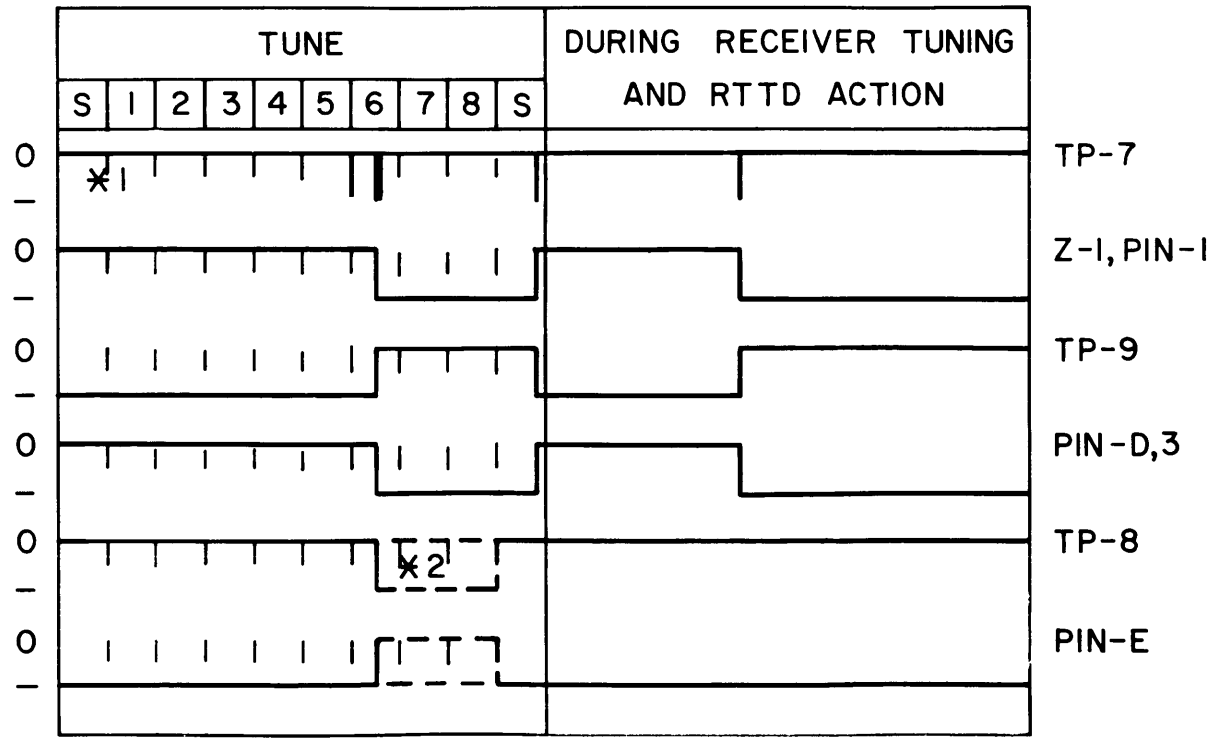


Figure 5-8. Timing Chart, Integrated Shift Register Card, A7 (Sheet 1 of 3)

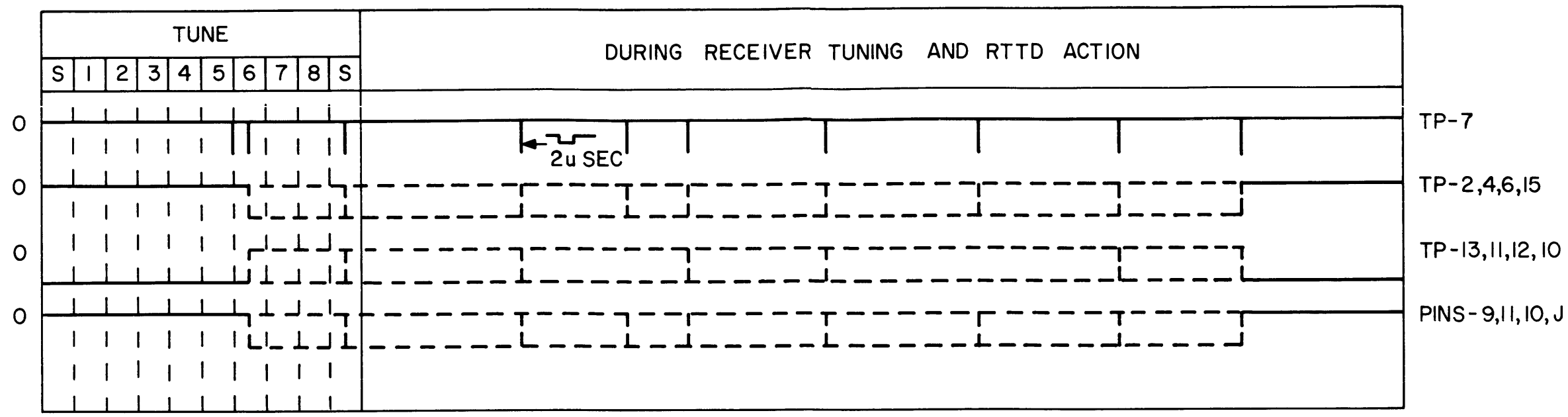




*NOTE: 1. The waveforms shown are representative of a particular program. The program used to generate these waveforms is, "changing the 10 mcs selector switch on the HFSR from position 0 to position 2". Any program will cause a series of shift pulses at TP-7. The waveforms will follow in coincidence with the shift pulses.

2. The waveforms shown in solid lines for the TUNE character are generated by the action of an RTTD when there is a program. With no program, the waveforms shown in broken lines will be present.

Figure 5-8. Timing Chart, Integrated Shift Register Card, A7 (Sheet 2 of 3)



NOTE: The incoming shift pulses are generated by the "Memory Advance" pulses from the RTTD as the ledexes in the RTTD and the receiver position themselves in accordance with the program. The signals in coincidence with the shift pulses change in accordance with the presence of Bits (no Bit-remains at static level, with a Bit-signal level changes from static level). Specific Bits are at the following test points:

BIT-2	TP-2	TP-13	PIN-9
BIT-3	TP-4	TP-11	PIN-11
BIT-4	TP-6	TP-12	PIN-10
BIT-5	TP-15	TP-10	PIN-J

Figure 5-8. Timing Chart, Integrated Shift Register Card, A7 (Sheet 3 of 3)

SECTION VI
PARTS LIST

6-1. INTRODUCTION

The parts list presented in this section is a cross-reference list of parts identified by a reference designation and TMC part number. In most cases, parts appearing on schematic diagrams are assigned reference designations in accordance with MIL-STD-16. Wherever practicable, the reference designation is marked on the equipment, close to the part it identifies. In most cases, mechanical and electro-mechanical parts have TMC part numbers stamped on them.

To expedite delivery when ordering any part, specify the following:

a. Reference symbol (For component parts of PC boards order as follows A-4569-C1)

b. Descriptions as indicated in parts list

c. TMC part number

d. Model and serial numbers of the equipment containing the part being replaced; this can be obtained from the equipment nameplate.

For replacement parts not covered by warranty (refer to warranty sheet in front of manual), address all purchase orders to:

The Technical Materiel Corporation
Attention: Sales Department
700 Fenimore Road
Mamaroneck, New York

Table 6-1 is a list of assemblies and subassemblies of the RTMU-41A and the page on which its parts list is located.

TABLE 6-1. ASSEMBLIES AND SUBASSEMBLIES

RTMU-41A CHASSIS

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
B1	BLOWER, FAN	BL131
C1	CAPACITOR, FIXED, ELECT: 2600 uf, 50 WVDC	CE112-6
C2	Same as C1	
C3	Same as C1	

RTMU-41A CHASSIS (Continued)

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
CR1	SEMICONDUCTOR DEVICE, DIODE	MIL1N2989RB
CR2	SEMICONDUCTOR DEVICE, RECTIFIER	RX108-2
DS1	LAMP, INCAND: Single contact, T-1-3/4 base, 28 v a-c or d-c	B1110-7
DS2	Same as DS1	
F1	FUSE, CARTRIDGE TYPE: 1 amp	FU102-1.00
F2	Same as F1	
SPARE	Same as F1	
FL1	FILTER, LINE	F1105-1
FL2	Same as FL1	
J1	CONNECTOR, RECEPTACLE, MALE	MS3102A14S1P
J3	CONNECTOR, RECEPTACLE, FEMALE	MS3102A32-414S
J4	CONNECTOR, RECEPTACLE, MALE	MS3102A20-27P
K1	RELAY, ARM, DPDT	RL178-06D5R2
MP1	FILTER, AIR	AO102-4
Q1	TRANSISTOR	MIL 2N3055
S1	SWITCH, TOGGLE: DPST	ST22K
T1	TRANSFORMER, POWER	TF0378
TB1	TERMINAL BD, BARRIER: 2-post, 6-32 thd	TM100-2
XA1	CONNECTOR, RECEPTACLE: P/C board, 22 double-sided female contacts	JJ319-22DFE
AX2	Same as XA1	
AX3	Same as XA1	
XA4	Same as XA1	
XA5	Same as XA1	
XA6	Same as XA1	
XA7	Same as XA1	
XA8	Same as XA1	
XA9	Same as XA1	
XA10	Same as XA1	
XA11	Same as XA1	

RTMU-41A CHASSIS (Continued)

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
XDS1	LIGHT, INDICATOR: translucent blue lens for T 1-3/4 lamp base	TS153-11
XDS2	LIGHT, INDICATOR: translucent white lens for T 1-3/4 lamp base	TS153-5
XF1	FUSE HOLDER, LAMP INDICATING	FH104-3
XF2	Same as XF1	
XK1	SOCKET, RELAY	TS195
XQ1	SOCKET, SEMICONDUCTOR DEVICE	TS166-1

A1, ISOLATION KEYER A4494

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
C1	CAPACITOR, FIXED, MICA	CN111F102D1S
C2	CAPACITOR, FIXED, ELECT	CL65BG101KP3
C3	Same as C2	
CR1	SEMICONDUCTOR DEVICE, DIODE	MIL1A4245
CR2	Same as CR1	
CR3	Same as CR1	
CR4	RECTIFIER, BRIDGE	DD130-200-1.5
K1	RELAY, ARM - SPDT	RL167-1
Q1	TRANSISTOR	MIL2N3013
R1	RESISTOR, FIXED, COMP	RC20GF472J
R2	RESISTOR, FIXED, COMP	RC32GF271J
R3	Same as R1	
R4	RESISTOR, VARIABLE, COMP	RV111-U-102A
R5	RESISTOR, FIXED, COMP	RC32GF101J
R6	RESISTOR, FIXED, COMP	RC32GF221J
TP1	TERM STUD	TEO127-2
TP2	Same as TP1	

A2, CLOCK TIMING CIRCUIT A4565

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
C1	CAPACITOR, FIXED, MTLZ	CN112A185J
C2	Same as C1	
C3	CAPACITOR, FIXED, MICA	CM112F152D5S
L1	COIL, RF, FIXED	CL275-102
R1	RESISTOR, FIXED, COMP	RC07GF472J
R2	RESISTOR, VARIABLE, COMP	RV121-1-501
R3	RESISTOR, FIXED, COMP	RC32GF331J
R4	RESISTOR, FIXED, COMP	RC07GF122J
R5	RESISTOR, FIXED, COMP	RC07GF392J
R6	Same as R4	
TP1	TERM STUD	TEO 127-2
TP2	Same as TP1	
TP3	Same as TP1	
TP4	Same as TP1	
TP5	Same as TP1	
TP6	Same as TP1	
TP7	Same as TP1	
TP8	Same as TP1	
TP9	Same as TP1	
TP10	Same as TP1	
TP11	Same as TP1	
TP12	Same as TP1	
TP13	Same as TP1	
Z1	NW DIG F/F	NW151
Z2	NW DIG/TIM/GEN	NW152
Z3	NW DIG SS GEN	NW153
Z4	NW DIG AND/GATE	NW142-24
Z5	NW DIG AND/GATE	NW142-43
Z6	Same as Z5	
Z7	Same as Z4	

A2, CLOCK TIMING CIRCUIT A4565 (Continued)

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
Z8	NW DIG INVERTER	NW150-4
Z9	Same as Z1	
Z10	Same as Z1	
Z11	Same as Z1	
Z12	NW EMIT FOL	NW147-2

A3, PARALLEL SHIFT - REGISTER A4566

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
C1	CAP., FXD, MICA	CM111F471F5S
TP1	TERM STUD	TEO 127-2
TP2	Same as TP1	
TP3	Same as TP1	
Z9	NW DIG AND/GATE	NW141-42
Z7	NW DIG AND/GATE	NW141-91
Z10	NW DIG AND/GATE	NW142-24
Z11	Same as Z10	
Z1	NW DIG F/F	NW151
Z2	Same as Z1	
Z3	Same as Z1	
Z4	Same as Z1	
Z5	Same as Z1	
Z6	Same as Z1	
Z8	Same as Z1	

A4, GATING CIRCUIT A4567

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
CR1	SEMICONDUCTOR DEVICE, DIODE	MIL1N914
CR2	Same as CR1	
CR3	Same as CR1	
CR4	Same as CR1	

A4, GATING CIRCUIT A4567 (Continued)

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
CR5	Same as CR1	
CR6	Same as CR1	
CR7	Same as CR1	
CR8	Same as CR1	
R1	RES, FXD, COMP	RC07GF102J
R2	Same as R1	
R3	Same as R1	
TP1	TERM STUD	TEO 127-2
TP2	Same as TP1	
TP3	Same as TP1	
TP4	Same as TP1	
TP5	Same as TP1	
TP6	Same as TP1	
TP7	Same as TP1	
TP8	Same as TP1	
TP9	Same as TP1	
TP10	Same as TP1	
TP11	Same as TP1	
TP12	Same as TP1	
TP13	Same as TP1	
TP14	Same as TP1	
TP15	Same as TP1	
TP16	Same as TP1	
TP17	Same as TP1	
TP18	Same as TP1	
TP19	Same as TP1	
TP20	Same as TP1	
TP21	Same as TP1	
TP22	Same as TP1	
TP23	Same as TP1	

A4, GATING CIRCUIT A4567 (Continued)

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
TP24	Same as TP1	
Z7	NW DIG AND/GATE	NW141-42
Z9	NW DIG AND/GATE	NW142-24
Z10	NW DIG AND/GATE	NW142-43
Z11	Same as Z10	
Z6	NW DIG INVERTER	NW150-4
Z8	Same as Z6	
Z1	NW DIG F/F	NW151
Z2	Same as Z1	
Z3	Same as Z1	
Z4	Same as Z1	
Z5	Same as Z1	

A6, SHIFT TIMING CIRCUIT A4569

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
C1	CAP, FXD, MTLZ	CN114-4R05J
C2	Same as C1	
C3	Cap, FXD, MICA	CM112F622G3S
C4	Same as C3	
C5	CAP., FXD, MICA	CM111F221G5S
C6	CAP., FXD, MICA	CM112F102D5S
CR1	SEMICONDUCTOR DEVICE, DIODE	MIL1N4245
CR2	SEMICONDUCTOR DEVICE, DIODE	MIL1N914
CR3	Same as CR2	
CR4	Same as CR2	
R1	RES, FXD, COMP	RC07GF102J
R2	RES, FXD, COMP	RC07GF473J
R3	Same as R1	
R4	RES, FXD, COMP	RC07GF182J

A6, SHIFT TIMING CIRCUIT A4569 (Continued)

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
R5	RES, FXD, COMP	RC07GF122J
R6	Same as R5	
R7	Same as R1	
TP1	TERM STUD	TEO 127-2
TP2	Same as TP1	
TP3	Same as TP1	
TP4	Same as TP1	
TP5	Same as TP1	
TP6	Same as TP1	
TP7	Same as TP1	
TP8	Same as TP1	
TP9	Same as TP1	
TP10	Same as TP1	
TP11	Same as TP1	
TP12	Same as TP1	
TP13	Same as TP1	
TP14	Same as TP1	
TP15	Same as TP1	
Z1	NW DIG TIME GEN	NW152
Z2	Same as Z1	
Z3	NW DIG INVERTER	NW150-4
Z4	Same as Z3	
Z5	NW DIG AND/GATE	
Z6	NW DIG AND/GATE	NW142-24
Z7	NW DIG SS GEN	NW153
Z8	NW DIG F/F	NW151
Z9	Same as Z3	
Z10	NW DIG COMP EM	NW147-2
Z11	Same as Z5	

A7, INTEGRATED SHIFT-REGISTER A4710

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
R1	RES, FXD, COMP	RC07GF102J
R2	Same as R1	
R3	Same as R1	
R4	Same as R1	
R5	Same as R1	
TP1	TERM STUD	TEO 127-2
TP2	Same as TP1	
TP3	Same as TP1	
TP4	Same as TP1	
TP5	Same as TP1	
TP6	Same as TP1	
TP7	Same as TP1	
TP8	Same as TP1	
TP9	Same as TP1	
TP10	Same as TP1	
TP11	Same as TP1	
TP12	Same as TP1	
TP13	Same as TP1	
TP14	Same as TP1	
TP15	Same as TP1	
Z6	NW DIG AND/GATE	NW141-42
Z11	NW DIG AND/GATE	NW142-24
Z7	NW DIG INVERTER	NW150-4
Z8	Same as Z7	
Z9	Same as Z7	
Z10	Same as Z7	
Z1	NW INTEG	NW175
Z2	Same as Z1	
Z3	Same as Z1	
Z4	Same as Z1	
Z5	Same as Z1	

A10, POWER SUPPLY A4549

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
C1	CAPACITOR, FIXED, ELECT	CE123-475-50B2
C2	CAPACITOR, FIXED, CER	CC100-44
C3	CAPACITOR, FIXED, MICA	CM111E470G5S
C4	CAPACITOR, FIXED, ELECT	CE123-475-35B2
C5	CAPACITOR, FIXED, ELECT	CE123-107-20S2
C6	Same as C3	
C7	Same as C4	
C8	Same as C3	
C9	CAPACITOR, FIXED, CERAMIC	CC100-44
CR1	RECTIFIER, BRIDGE	DD130-200-1.5
CR2	Same as CR1	
Q1	TRANSISTOR	MIL2N1485
Q2	TRANSISTOR	MIL2N4036
Q3	Same as Q2	
Q4	Same as Q1	
Q5	Same as Q2	
R1	RESISTOR, FIXED, COMP	RC32GF222J
R2	RESISTOR, FIXED, COMP	RC07GF6R8J
R3	RESISTOR, FIXED, COMP	RC20GF680J
R4	RESISTOR, FIXED, COMP	RC20GF560J
R5	RESISTOR, FIXED, FILM	RN60D3902F
R6	RESISTOR, FIXED, COMP	RC20GF122J
R7	RESISTOR, FIXED, COMP	RC20GF361J
R8	Same as R4	
R9	Same as R3	
R10	RESISTOR, FIXED, FILM	RN60D1802F
R11	Same as R3	
R12	Same as R4	
R13	RESISTOR, FIXED, COMP	RC20GF821J
R14	RESISTOR, FIXED, COMP	RC07GF470J

A10, POWER SUPPLY A4549 (Continued)

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
R15	RESISTOR, FIXED, COMP	RC42GF101J
R16	RESISTOR, FIXED, COMP	RC20GF242J
R17	RESISTOR, FIXED, FILM	RN60D2401F
R18	RESISTOR, FIXED, FILM	RN60D2701F
R19	RESISTOR, FIXED, COMP	RC20GF1R0J
R20	Same as R19	
R21	Same as R19	
R22	Same as R19	
R23	Same as R10	
R24	RESISTOR, FIXED COMP	RC20GF4R7J
R25	Same as R18	
R26	RESISTOR, FIXED, COMP	RC20GF102J
R27	RESISTOR, FIXED, WIRE WOUND, 5 watt	RR114-1W
R28	RESISTOR, FIXED, COMP	RC20GF272J
R29	Same as R19	
Z1	REGULATOR, VOLTAGE	VR104
Z2	Same as Z1	
Z3	Same as Z1	

A11, READBACK SELECTOR AX5009

REF SYMBOL	NAME AND DESCRIPTION	TMC PART NUMBER
CR1	SEMICONDUCTOR DEVICE, DIODE	2N1776A
CR2	SEMICONDUCTOR DEVICE, DIODE	MIL1N914
J2	CONNECTOR, RECP, FML	MS3102H-32-414S
R1	RESISTOR, FIXED, 2.2K, 1/4 W	2C07GF2225
S1	SWITCH, STEPPING	SW515

SECTION VII
DRAWINGS

7-1. INTRODUCTION

This section contains schematic diagrams for the RTMU-41A. Table 7-1 lists the figure numbers contained herein and the corresponding TMC drawing numbers.

TABLE 7-1. LIST OF DIAGRAMS

Figure No.	Title
7-1	Memory Bank Assembly
7-2	Schematic Diagram of Isolation Keyer A1
7-3	Schematic Diagram of Clock Timing Circuit A2
7-4	Schematic Diagram of Parallel Shift-Register A3
7-5	Schematic Diagram of Gating Circuit A4
7-6	Schematic Diagram of Shift Timing Circuit A6
7-7	Schematic Diagram of Integrated Shift-Register A7
7-8	Schematic Diagram of Power Supply Circuit A10
7-9	Schematic Diagram of Rotary Switch A11

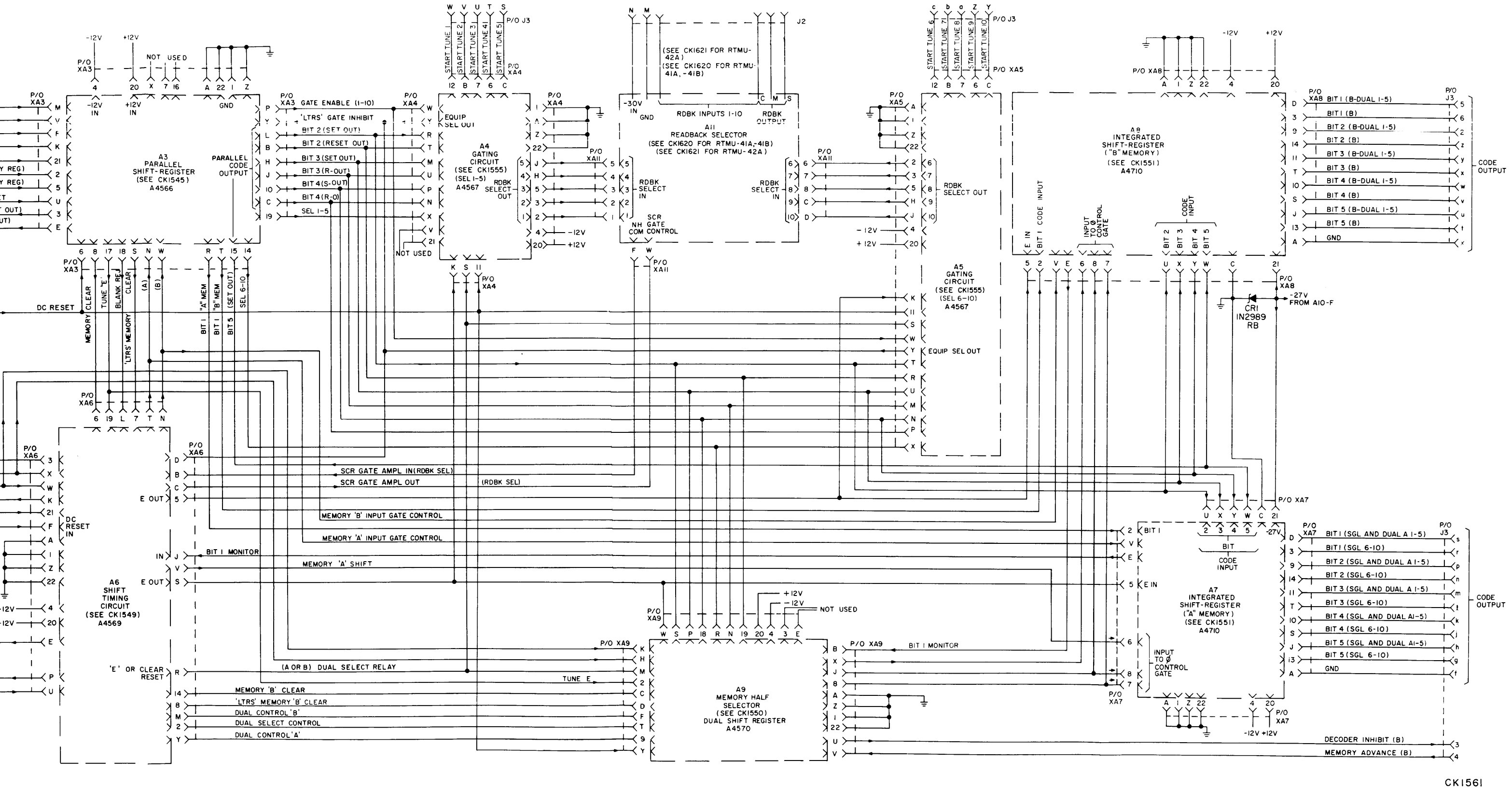
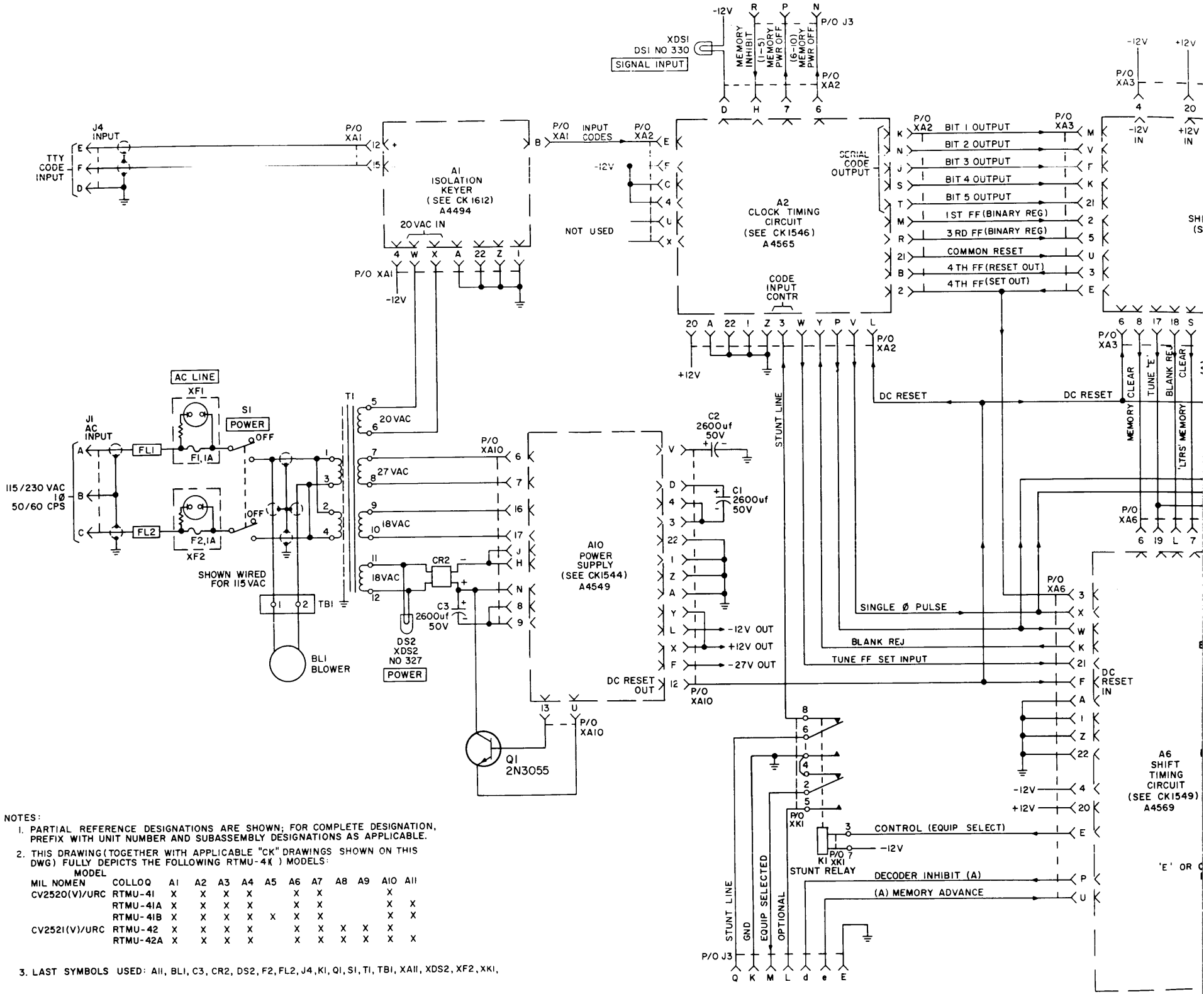


Figure 7-1. Memory Bank Assembly

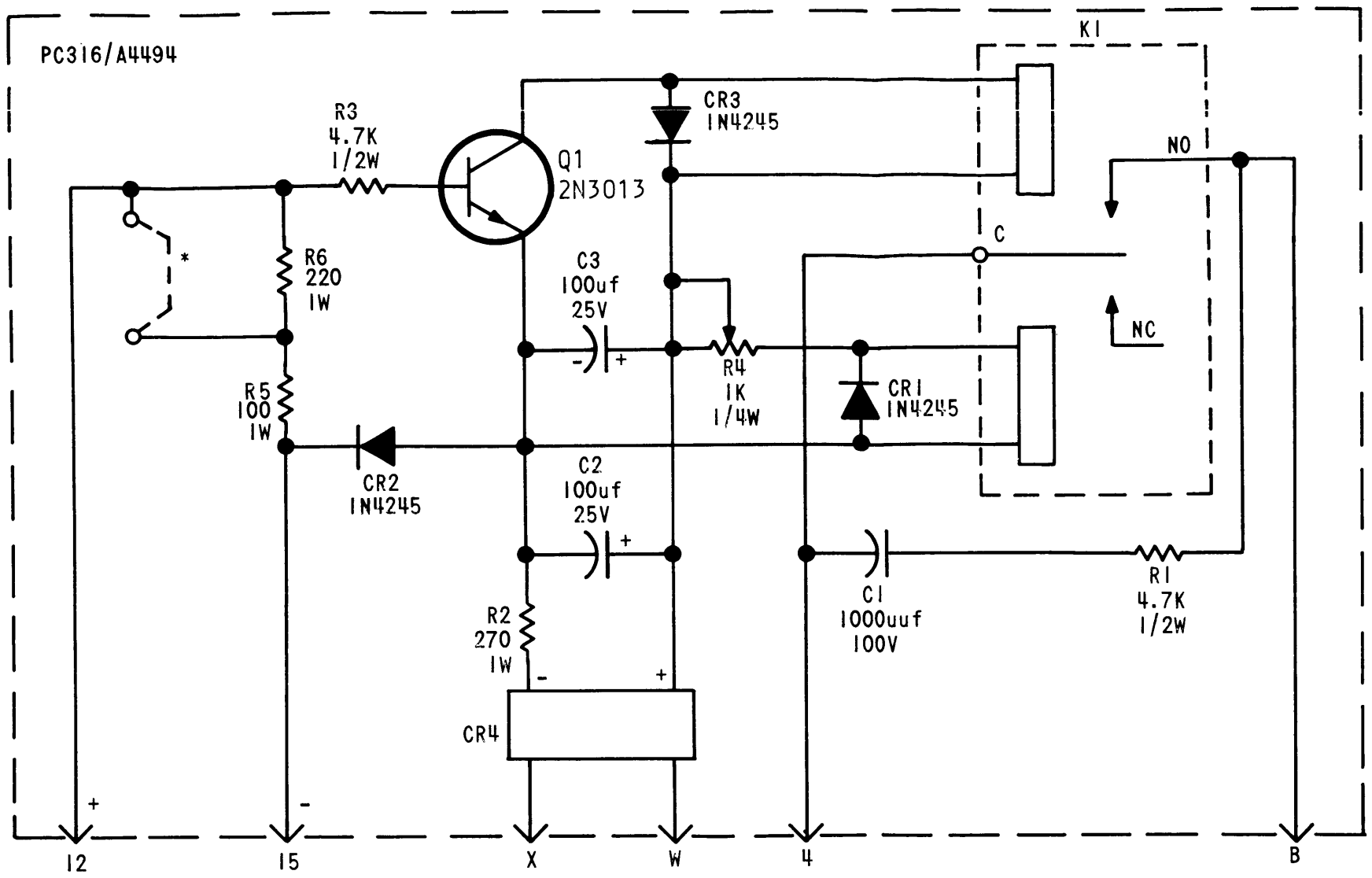


NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATIONS AS APPLICABLE.
2. THIS DRAWING (TOGETHER WITH APPLICABLE "CK" DRAWINGS SHOWN ON THIS DWG) FULLY DEPICTS THE FOLLOWING RTMU-4( ) MODELS:

MODEL MIL NOMEN	COLLOQ	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
CV2520(V)/URC	RTMU-41	X	X	X	X		X	X			X	
	RTMU-41A	X	X	X	X		X	X			X	X
	RTMU-41B	X	X	X	X	X	X	X			X	X
CV2521(V)/URC	RTMU-42	X	X	X	X		X	X	X	X	X	
	RTMU-42A	X	X	X	X		X	X	X	X	X	X

3. LAST SYMBOLS USED: A11, BL1, C3, CR2, DS2, F2, FL2, J4, K1, Q1, S1, T1, TB1, XA11, XDS2, XF2, XK1,



LAST SYMBOL	MISSING SYMBOL
R6 C3 CR4 K1 Q1	

NOTES

1. PARTIAL REFERENCE DESIGNATIONS AS SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION (S) AS APPLICABLE
* 2. STRAP IS INCLUDED WHEN 60mA LOOP IS USED STRAP IS NOT INCLUDED WHEN 20mA OR 6 VOLT LOOPS ARE USED.

CK1612

Figure 7-2. Schematic Diagram of Isolation Keyer A1

12

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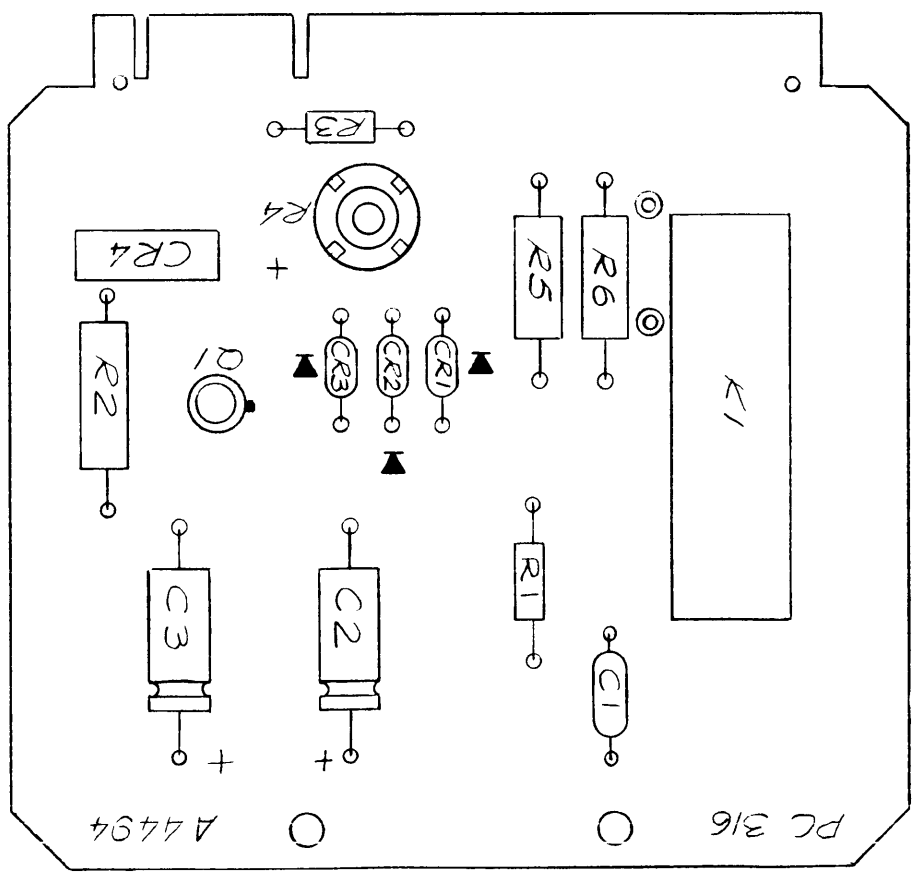
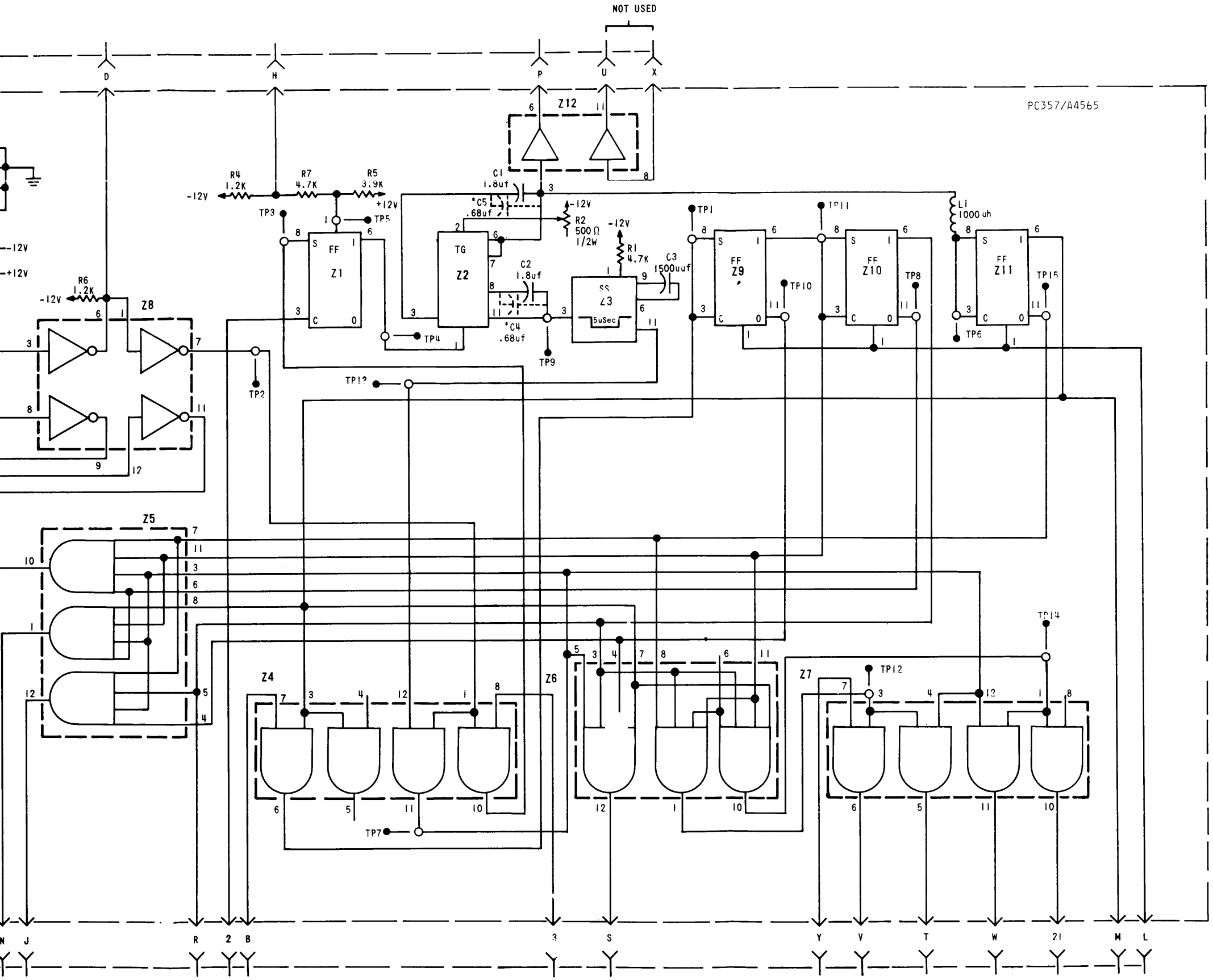


PC316



MODULE VOLTAGE AND GND CHART

SYMBOL	PIN CONNECTIONS		
	+12V	-12V	GND
Z1,3,9,10,11,	10	2	5
Z4,5,6,7		2	
Z2,8	10		5
Z12		2	5

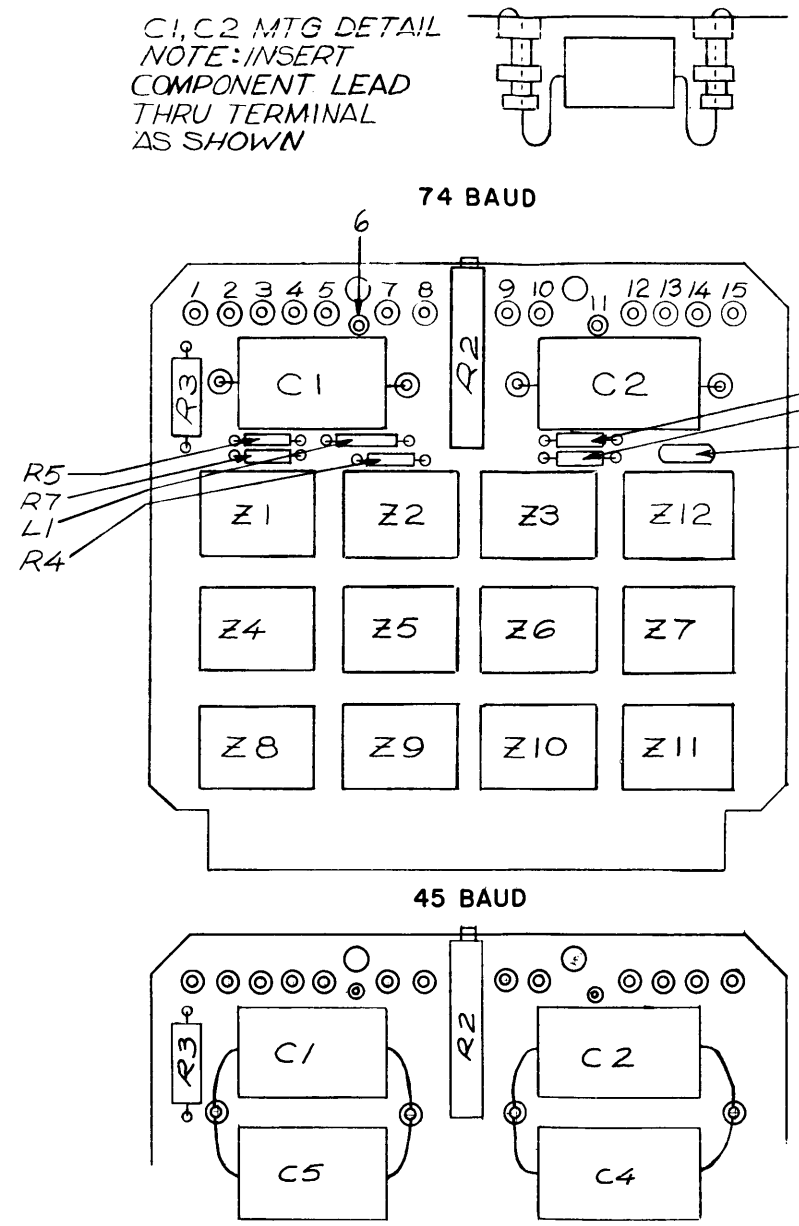
LAST SYMBOL	MISSING SYMBOL
C5 L1 R7 TP15 Z12	

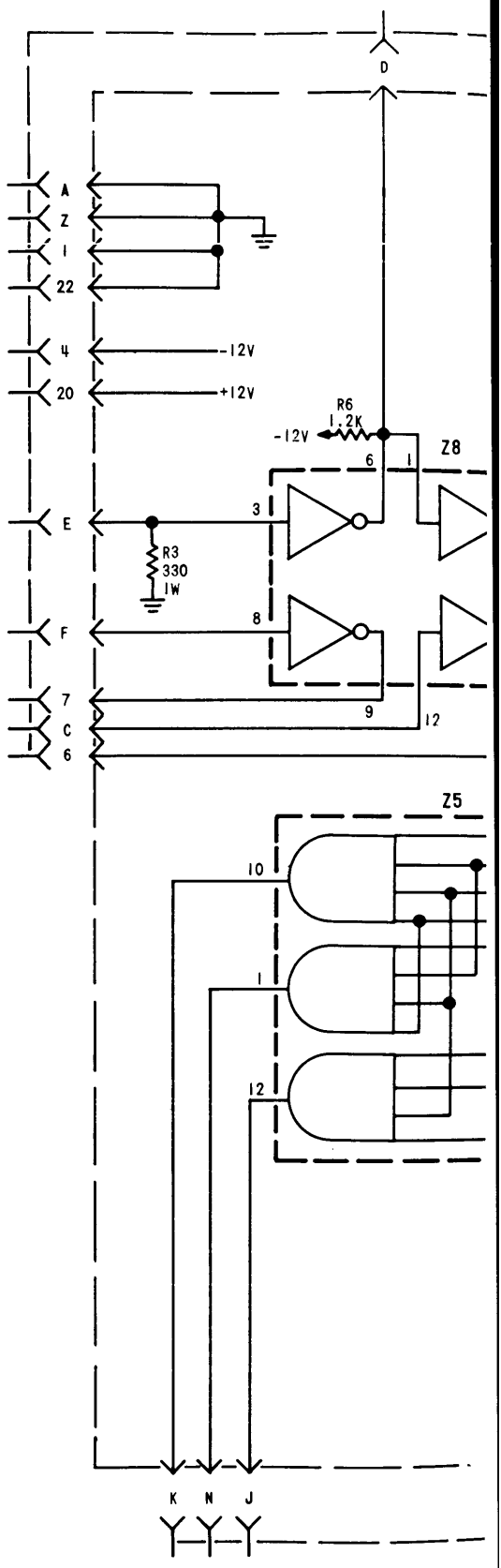
UNLESS OTHERWISE SPECIFIED:

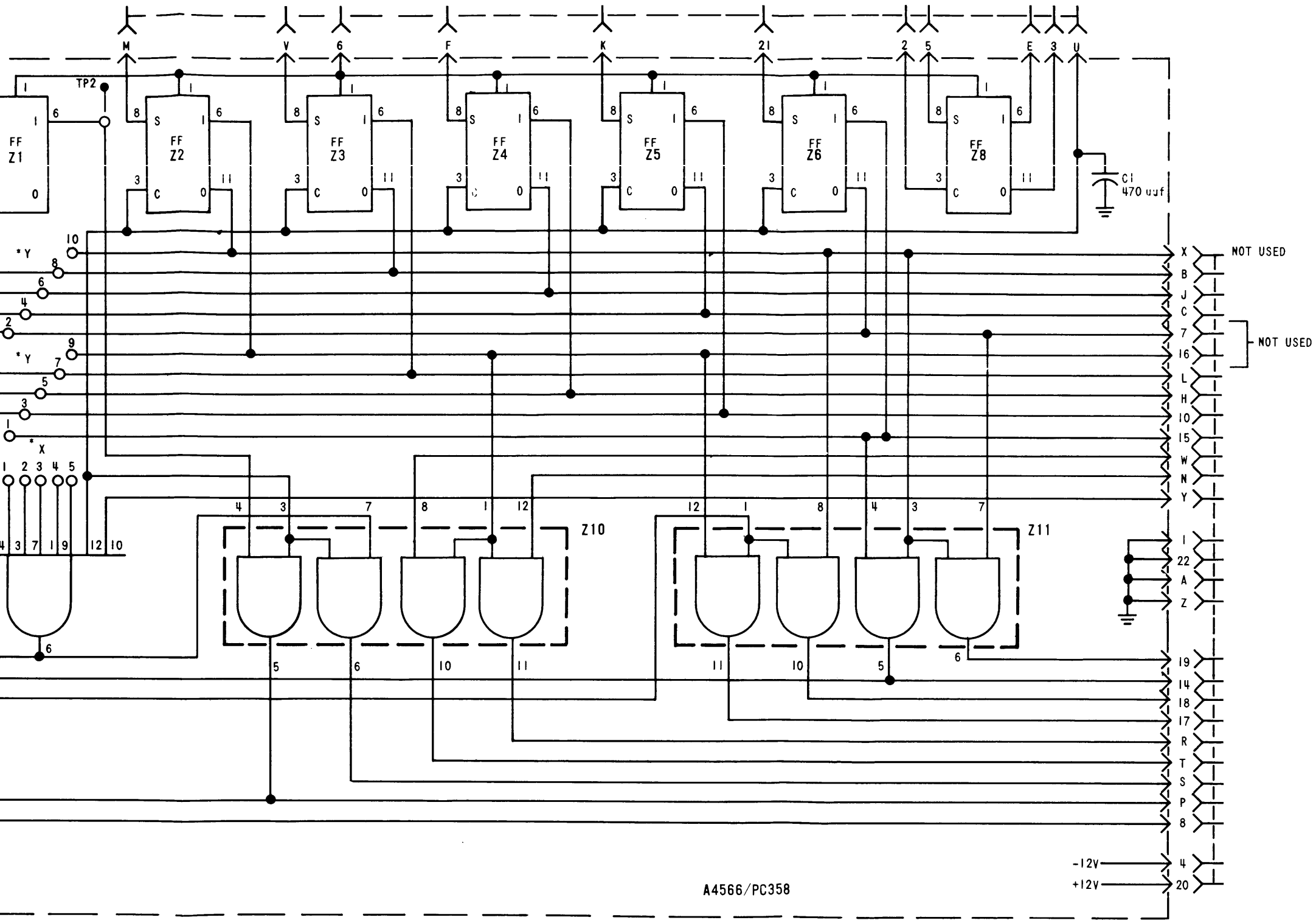
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4w.
2. * FOR 100 WPM DELETE C4 AND C5
   FOR 60 WPM ADD C4 AND C5
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION (S) AS APPLICABLE

CK1546

Figure 7-3. Schematic Diagram of Clock Timing Circuit A2


C1, C2 MTG DETAIL
NOTE: INSERT
COMPONENT LEAD
THRU TERMINAL
AS SHOWN
74 BAUD
6
1 2 3 4 5 7 8
9 10 11 12 13 14 15
R3
C1
R2
C2
R6
R1
C3
R5
R7
L1
R4
Z1
Z2
Z3
Z12
Z4
Z5
Z6
Z7
Z8
Z9
Z10
Z11
45 BAUD
R3
C1
R2
C2
C5
C4


D
A
Z
1
22
4
20
-12V
+12V
R6
1.2K
-12V
Z8
6
1
3
E
R3
330
1W
8
F
7
C
6
9
12
Z5
10
1
12
K
N
J



MODULE VOLTAGE & GND CHART

SYMBOL	PIN CONNECTIONS		
	+12V	-12V	GND
Z1 THRU Z6, Z8	10	2	5
Z10, Z11		2	
Z7		2	
Z9		2	

LAST SYMBOL	MISSING SYMBOL
C1 TP3 Z11	

*EQUIPMENT SELECTION JUMPER GUIDE

EQUIPMENT	JUMPER X				
	1	2	3	4	5
A	Y1	Y4	Y5	Y8	Y9
B	Y1	Y4	Y5	Y7	Y10
C	Y1	Y3	Y6	Y7	Y10
D	Y1	Y3	Y6	Y8	Y9
E	Y1	Y4	Y6	Y7	Y9

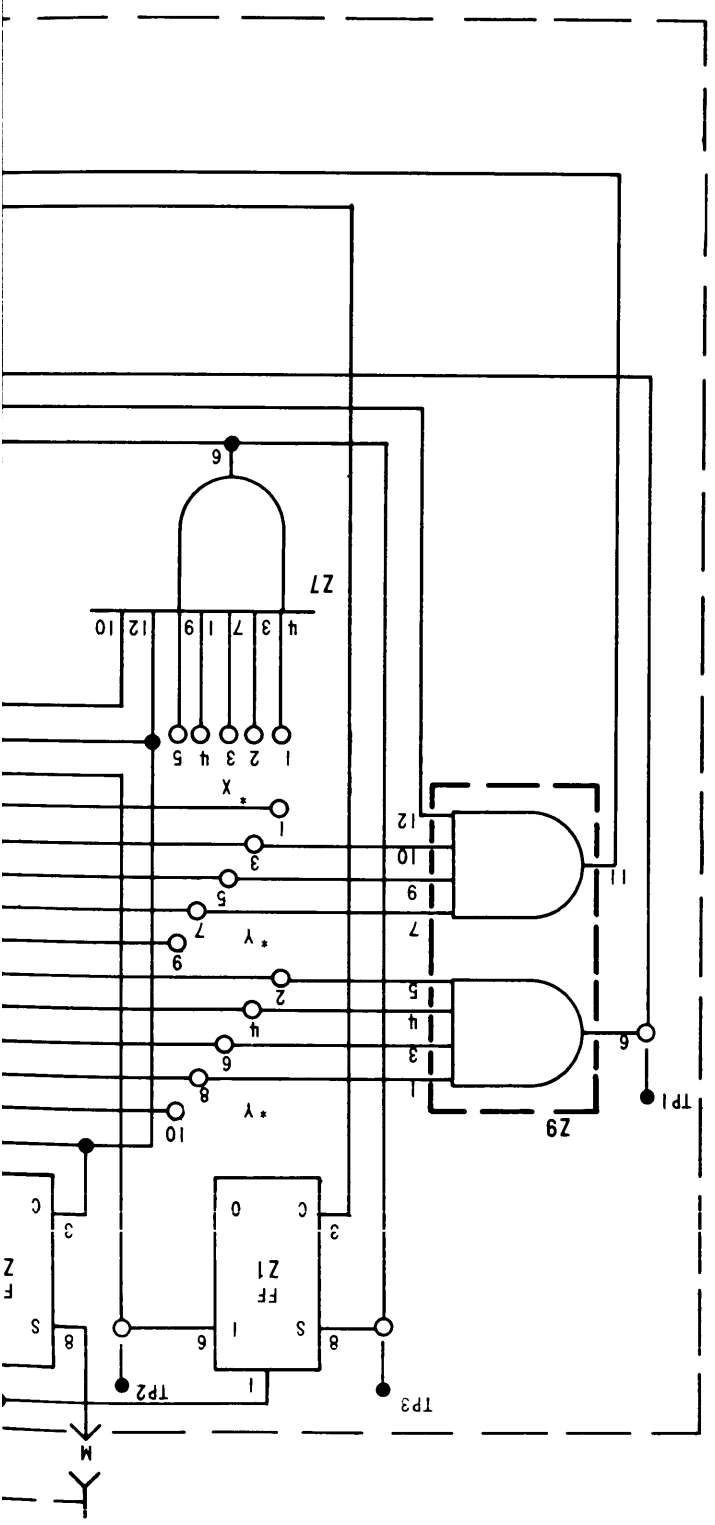
DESIGNATIONS ARE SHOWN; FOR COMPLETE
X WITH UNIT NUMBER AND SUB-ASSEMBLY
APPLICABLE

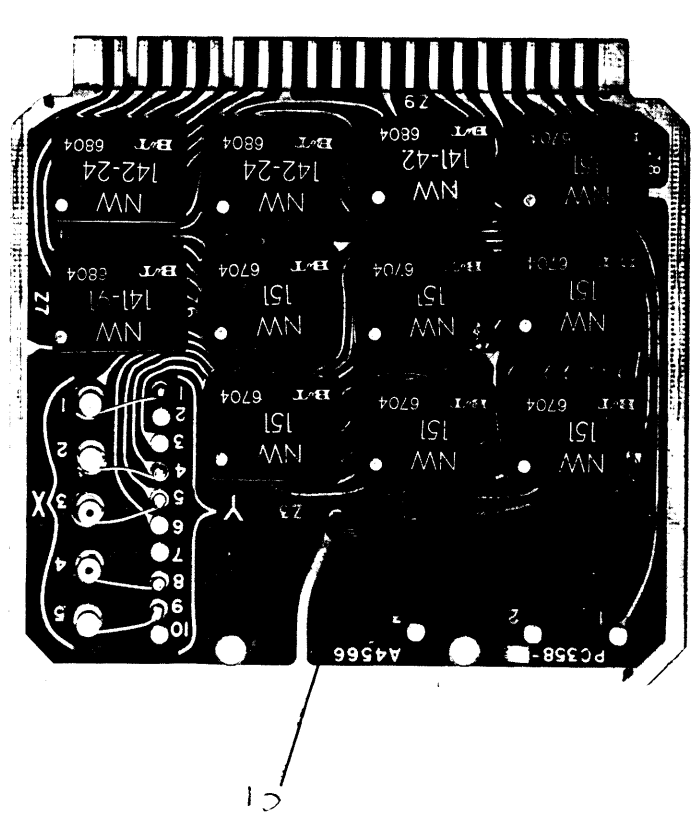
CK1545

Figure 7-4. Schematic Diagram of Parallel Shift Register A3

NOTE:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-DESIGNATION (S) AS APPLICABLE





MODULE VOLTAGE AND GND CHART

SYMBOL	PIN CONNECTIONS		
	+12V	-12V	GND
Z1 THRU Z5	10	2	5
Z6, Z8	10		5
Z7,Z9,Z10,Z11		2	

LAST SYMBOL	MISSING SYMBOL
CR8 R3 TP24 Z11	

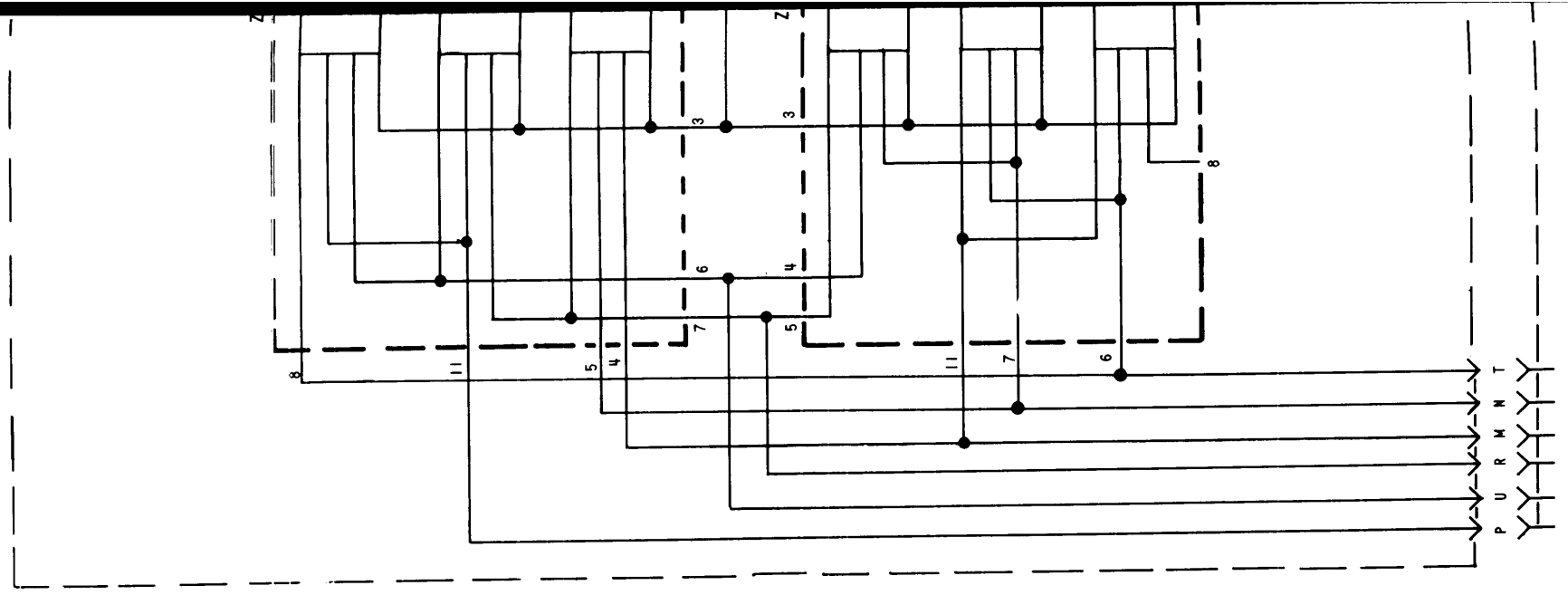
UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W.
2. ALL DIODE VALUES ARE IN914
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION (S) AS APPLICABLE

A4567/PC359

CKI555

Figure 7-5. Schematic Diagram of Gating Circuit A4


Z7
Z2
Z1
Z10
R3
Z4
Z8
A4567
PC359
NW 151
NW 141-42
NW 142-43
NW 150-4
NW 142-24

MODULE VOLTAGE AND GND CHART

SYMBOL	PIN CONNECTIONS		
	+ 12V	-12V	GND
Z1.Z2.Z7.Z8	10	2	5
Z3.Z4.Z9	10		5
Z5.Z6.Z11		2	
Z10		2	5

LAST SYMBOL	MISSING SYMBOL
C6	
CR4	
TP15	
Z11	
R7	

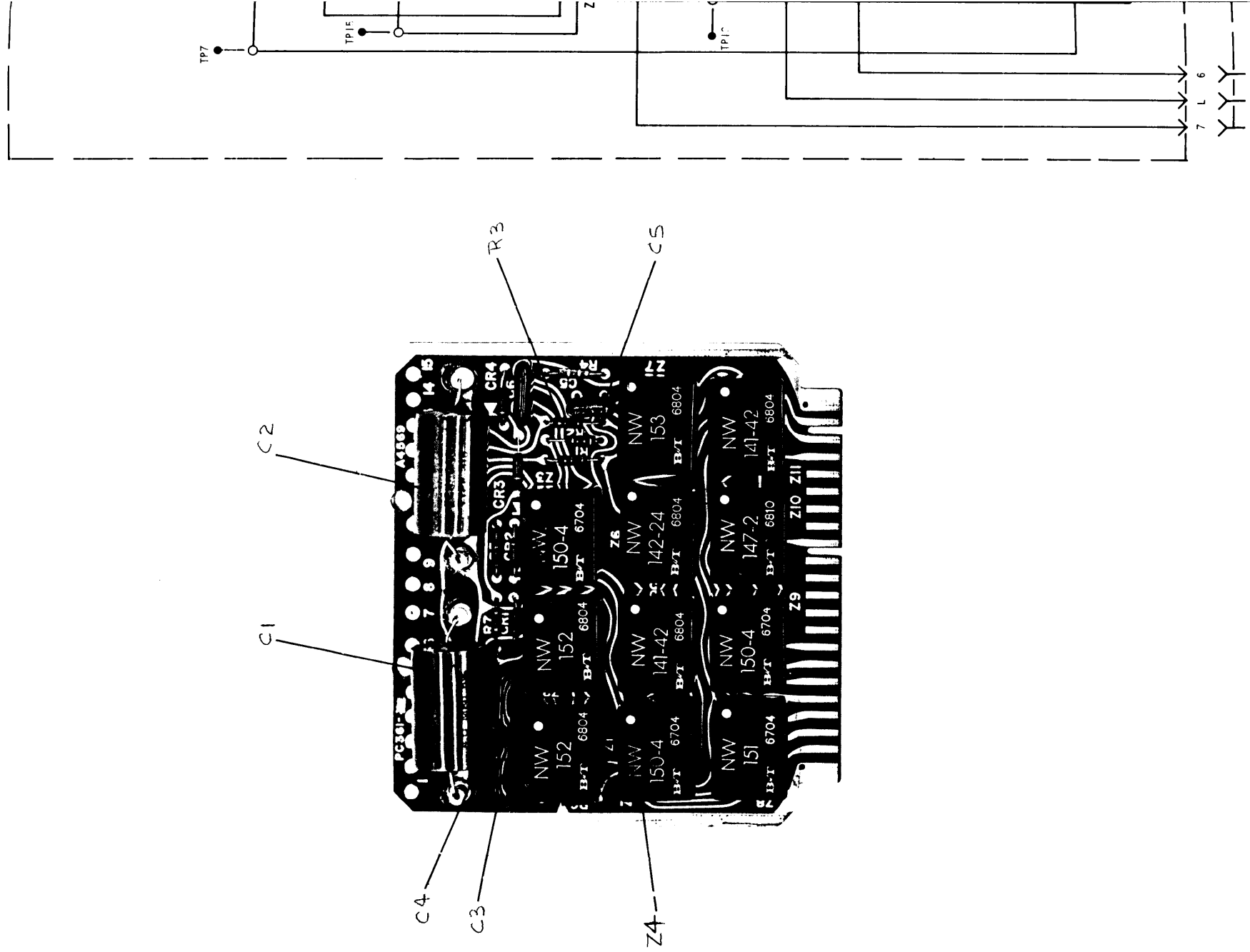
UNLESS OTHERWISE SPECIFIED:

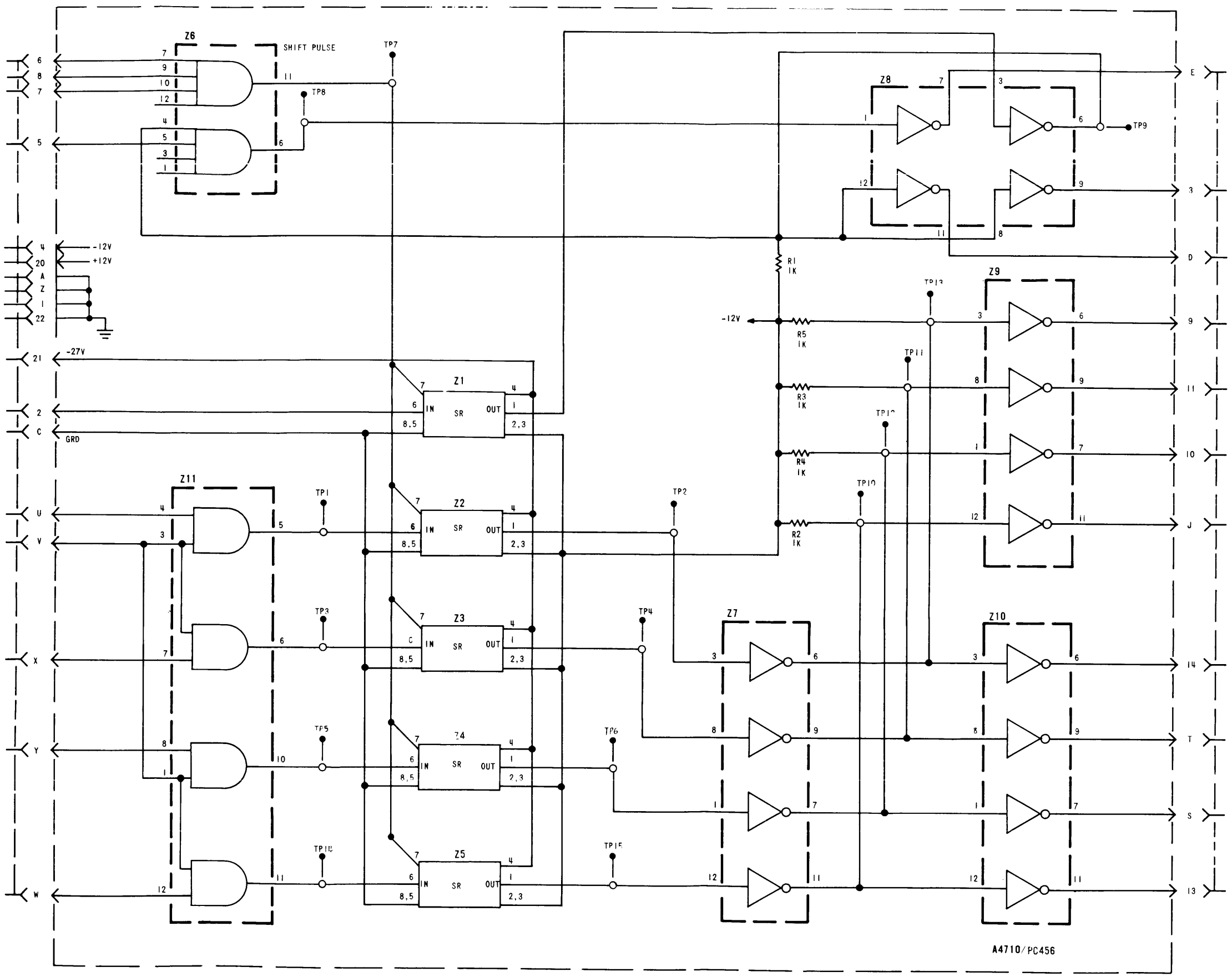
1. ALL RESISTOR VALUES ARE IN OHMS. 1/4W
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE

A4569/PC361

CKI549

Figure 7-6. Schematic Diagram of Shift Timing Circuit A6


TP7
TP15
TP1
7 L 6
R3
C5
C2
C1
C4
C3
Z4
A1B9
CR4
CR3
Z6
Z9
Z10
Z11
Z7
Z8
NW
B-T
6804
6704
6810
150-4
152
141-42
142-24
147-2
153
151



MODULE VOLTAGE & GND CHART

SYMBOL	PIN CONNECTIONS			
	+12V	-12V	GND	-27V
Z1 THRU Z5		2,3	5,8	4
Z6, Z11		2		
Z7,Z8,Z9,Z10	10		5	

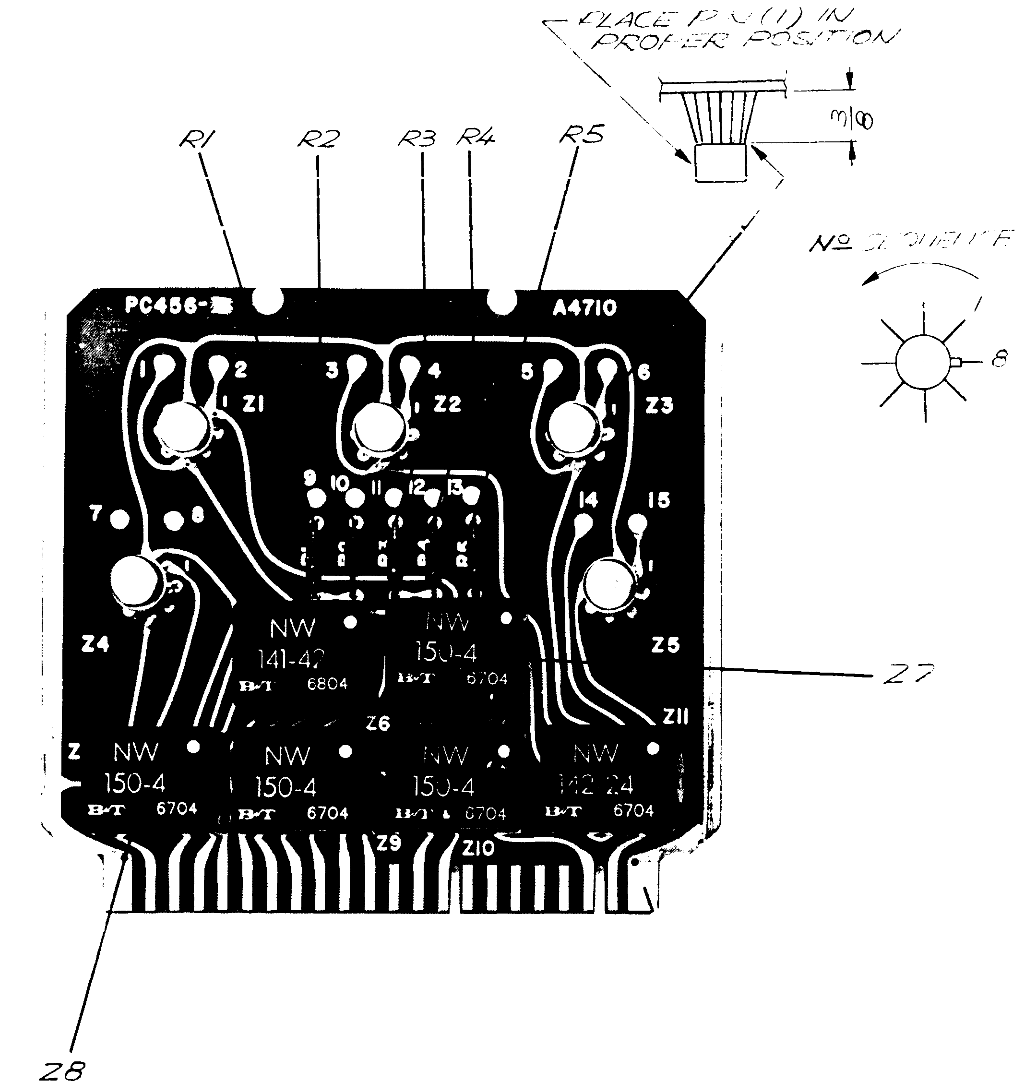
LAST SYMBOL	MISSING SYMBOL
R5 TP15 Z11	

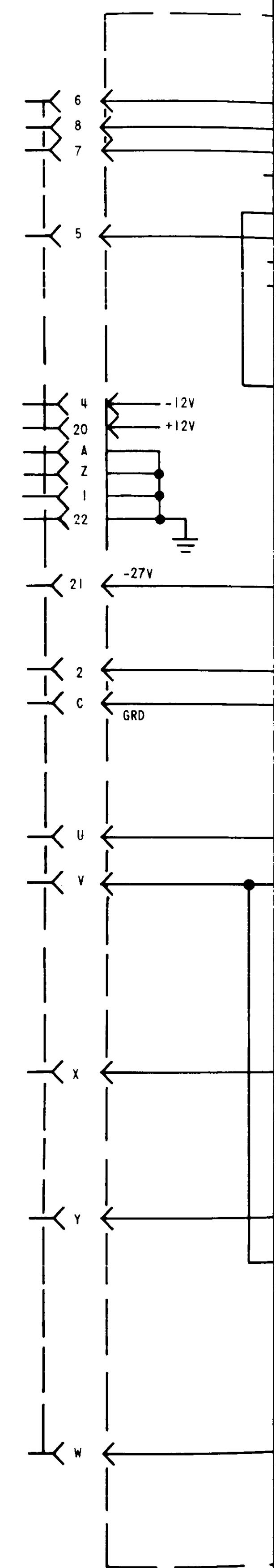
UNLESS OTHERWISE SPECIFIED:

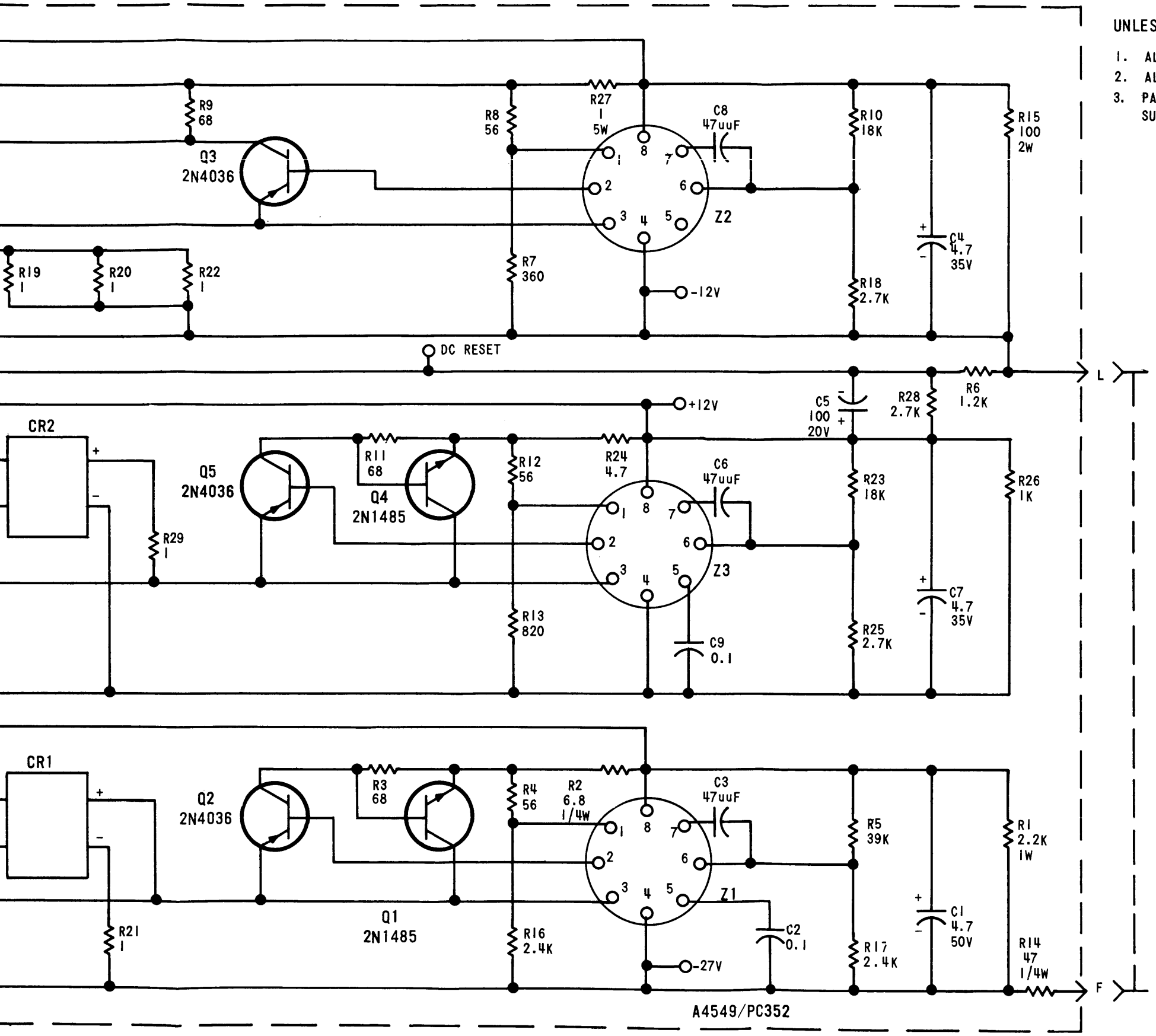
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION (S) AS APPLICABLE

CK1551

Figure 7-7. Schematic Diagram of Shift-Register A7


PLACE P.C.(1) IN PROPER POSITION
3/8
R1
R2
R3
R4
R5
PC456
A4710
Z1
Z2
Z3
Z4
Z5
Z6
Z7
Z8
Z9
Z10
Z11
NW 141-42 B-T 6804
NW 150-4 B-T 6704
NW 142-24 B-T 6704


6
8
7
5
4
20
A
Z
1
22
-12V
+12V
21
-27V
2
C
GRD
U
V
X
Y
W



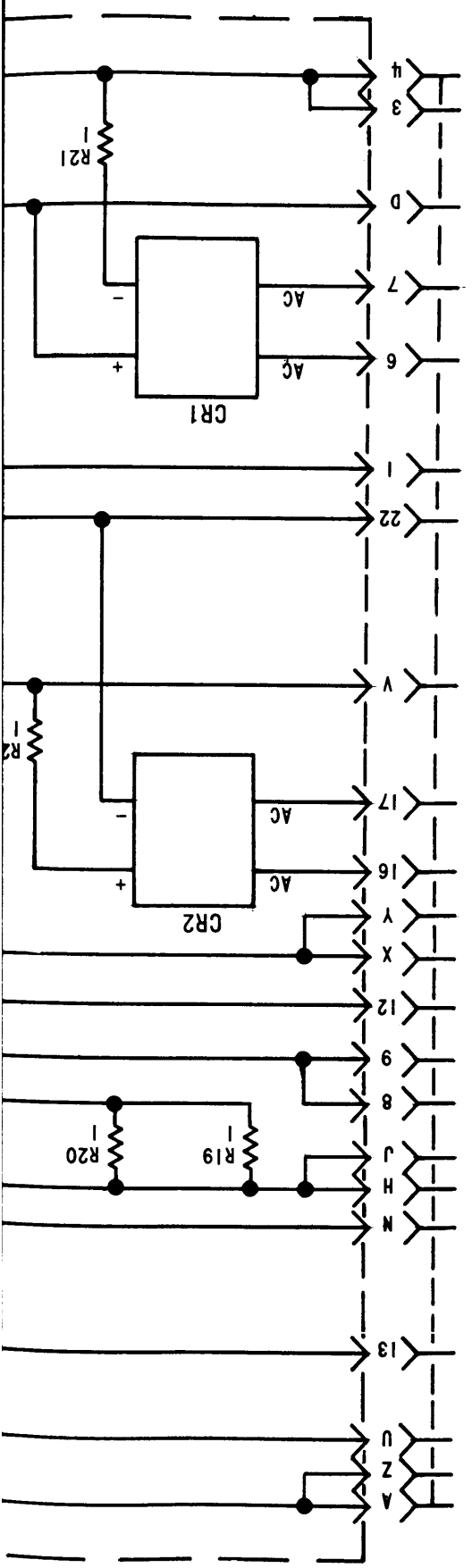
UNLESS OTHERWISE SPECIFIED:

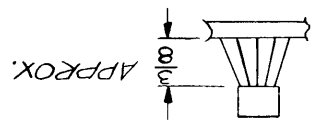
1. ALL RESISTOR VALUES ARE IN OHMS, 1/2 WATT.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. PARTIAL REFERENCE DESIGNATION ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE.

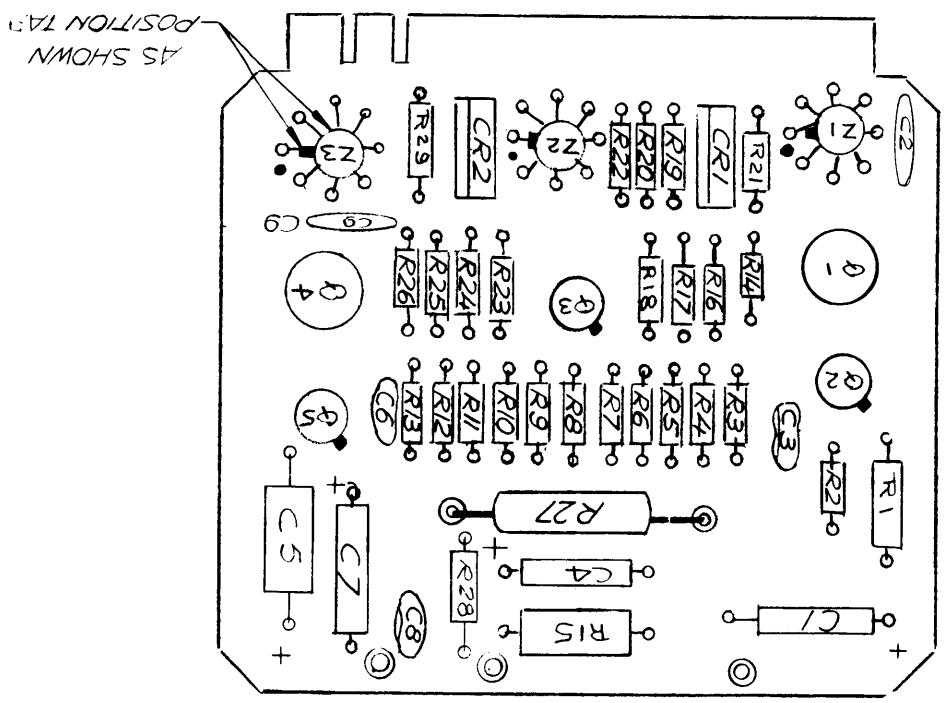
LAST SYMBOL	MISSING SYMBOL
C9	
CR2	
Q5	
R29	
Z3	

CK1544

Figure 7-8. Schematic Diagram of Power Supply A10


4
3
R21
D
7
AC
6
AC
CR1
1
22
V
17
AC
16
AC
CR2
Y
X
12
9
8
R19
R20
J
H
N
13
U
Z
A


APPROX.
.010


AS SHOWN
POSITION TAB
Z3
CR2
Z2
CR1
Z1
C2
C9
Q4
Q3
Q1
Q2
S5
C6
C3
C5
C7
C8
R27
C4
R15
C1
R28
R22
R1

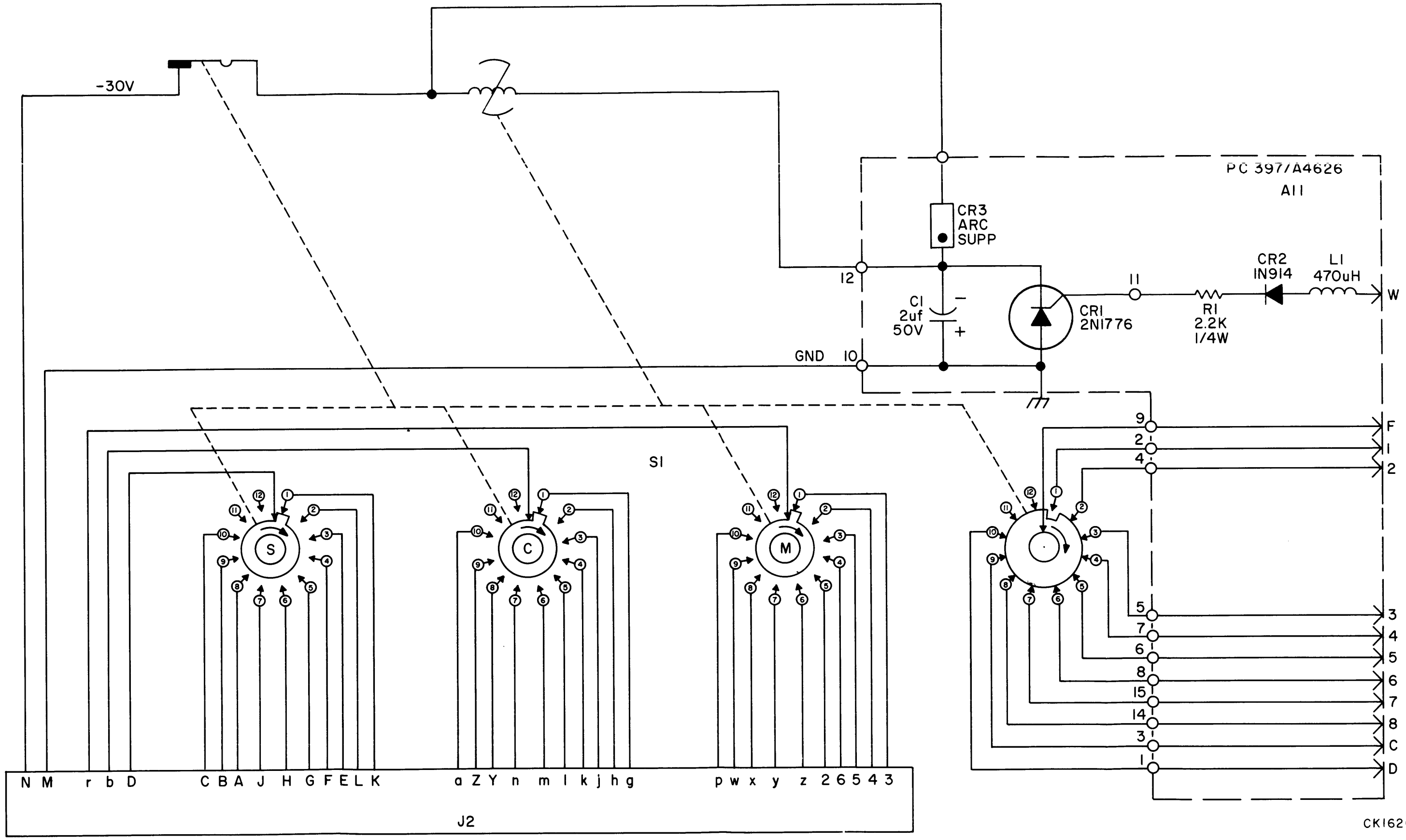


Figure 7-9. Schematic Diagram of Rotary Switch A11