UNCLASSIFIED

NAVELEX 0967-385-1010

TECHNICAL MANUAL

for

COMMUNICATION CONTROL CONSOLE AN/URA-63

DEPARTMENT OF THE NAVY
NAVAL ELECTRONIC SYSTEMS COMMAND

UNCLASSIFIED

Publication: 23 NOVEMBER 1970

LIST OF EFFECTIVE PAGES

TECHNICAL MANUAL NAVELEX 0967-385-1010

PAGE NUMBERS	CHANGE IN EFFECT	PAGE NUMBERS	CHANGE IN EFFECT
Title Page	Original	4-0 to 4-24	Original
ii to v	Original	5-1 to 5-86	Original
1-0 to 1-9	Original	6-1 to 6-15	Original
2-0 to 2-7	Original	i-0 to i-2	Original

OPERATORS HANDBOOK NAVELEX 0967-385-1020

PAGE NUMBERS	CHANGE IN EFFECT	PAGE NUMBERS	CHANGE IN EFFECT
Title Page	Original	3-1 to 3-8	Original
ii to v	Original		

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MAMARONECK, NEW YORK 10543

CONTRACT N00039-66-C-0161

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

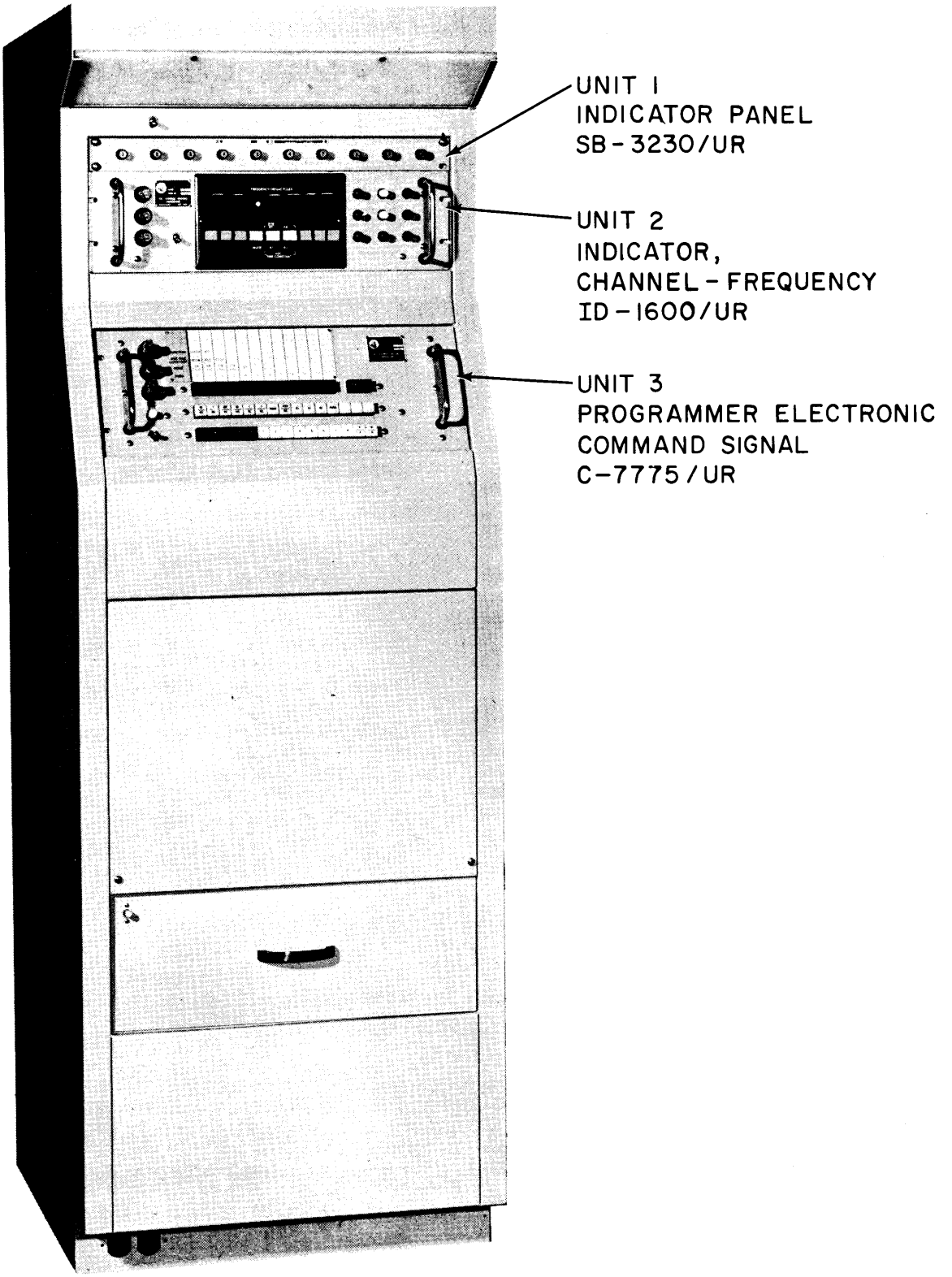


Figure 1-1. Communication Control Console, AN/URA-63

SECTION 1

GENERAL INFORMATION

1-1. SCOPE.

This Technical Manual is in effect upon receipt, and supersedes any previous or preliminary information. Extracts from this publication released prior to the issue date of this text may be made to facilitate the preparation of other Department of Defense publications.

The context of this manual covers Communication Control Console, AN/URA-63 as used in association with Radio Receiving Sets AN/URR-63(V)1 and AN/URR-63(V)2.

1-2. GENERAL DESCRIPTION (See Figure 1-1).

Communication Control Console AN/URA-63 is a control programming and monitoring unit for the remote teletype signal control of Radio Receiving Sets AN/URR-63(V)1 and AN/URR-63(V)2. Remote tuning of the receiver is accomplished by programming receiver control settings on a pushbutton keyboard. The 5-level binary codes generated from the keyboard reach the receiver memory (code storage) section via associated teletype linkage. A readback indicator in the AN/URA-63 receives receiver control position readback codes, in similar coding, from teletype linkage, and displays the settings by digital indicators and projection screens.

The AN/URA-63 may be used for remote control and monitoring of a series of AN/URR-63(V)1 and/or AN/URR-63(V)2 receivers, using the same programmer and readback indicator. Equipment selection buttons on the programmer (in five letters and ten numerals) can be combined to select and tune up to 50 receivers. This arrangement is for five groups of receivers, each group can contain either ten single receivers, or five dual diversity receivers. A light indicator display works with the readback indicator to reveal which receiver is associated with the current control position readback.

The AN/URA-63 comprises modular units (described in paragraph 1-3) mounted in a sloped front cabinet. All circuitry is a solid state design, with encapsulated binary logic modules on printed circuit plug-in cards throughout. The overall cabinet dimensions are 65 inches high by 22 inches wide by 24 inches deep and the weight of the complete assembly is approximately 193 lbs. The programmer and readback units are on tilt-lock slides and lock in the up or down position for servicing and these units contain their own power supplies. Forced-air cooling systems with removable air filters are incorporated where cooling is required. Cabinet and units are finished in light gray enamel per MIL-E-15090.

1-3. DESCRIPTION OF MODULAR UNITS.

a. ELECTRONIC COMMAND SIGNAL PROGRAMMER, C-7775/UR. - The C-7775/UR contains the pushbutton keyboard marked with receiver controls for composing a teletype tuning message to be sent to the receiver. It includes a CLEAR button to correct errors and a TUNE button to initiate positioning of the receiver tuning controls. A row of EQUIPMENT SELECTION buttons are included and provide a selection of five 10- receiver groups for address. The contact keying output is in a CCIT-8-level start-and-stop teletype pattern at a 74.2- baud rate, with intelligence carried within the first five levels.

b. CHANNEL/FREQUENCY INDICATOR, ID-1600/UR. - The ID-1600/UR displays a receiver status readback from a continuous cyclic sampling of receiver control positions, transmitted as 8-level teletype codes from the receiver. Code input is through an isolation keyer and can be connected directly to any standard teletype current loop in 5-level through 8-level equipments at a 74.2 baud rate. The frequency to which the receiver is tuned appears in a lighted digital display down to the .0001-mc component. Control positions are projected onto individual indicator screens. Receiver status and warning signals are on a light panel.

c. INDICATOR PANEL SB-3230/UR. - The SB-3230/UR is a light indicator panel operating in conjunction with Channel/Frequency Indicator ID-1600/UR to identify which receiver (of a group of receivers) is represented in the ID-1600/UR display. Lights enable an identification of up to ten receivers. The SB-3230/UR is a passive device and works from a signal input from Channel/Frequency Indicator ID-1600/UR.

1-4. REFERENCE DATA.

Table 1-1 lists quick-reference technical data on the Communication Control Console and includes the nominal specifications defining this equipment. Table 1-2 lists teletype output codes for receiver controls, resulting from specific buttons on the C-7775/UR keyboard. Table 1-3 lists readback code inputs required to energize specific displays in the ID-1600/UR indicator panel.

TABLE 1-1. TECHNICAL SPECIFICATIONS

Tuning code output:	5-bit codes in serial teletype dry contact keying from polar relay. 8-level codes* with 74.2-baud rate. Codes per table 1-2.
Readback code input:	From teletype loop, 60 ma or 20 ma, neutral or polar. 5-level codes (adaptable up to 8-level* transmission equipment) with 74.2-baud transmission speed. Codes per table 1-3.
Power supply requirements:	115/230 vac, 50/60 cps, single phase, 168 watts maximum consumption.
Ambient temperature and humidity:	0 to 50°C and up to 95% relative humidity.
Overall dimensions:	65 inches high x 22 inches wide x 24 inches deep.
Weight:	193 lbs.

*In 6-, 7- or 8- level pattern, code is in first 5 bits.

TABLE 1-2. PUSHBUTTON CODES

PUSHBUTTON (C-7775/UR, Figure 3-1)	5-BIT CODE, 12345	EQUIVALENT CCIT TTY CHARACTER
FUNCTION:		
SYNTH	01000	Line Feed
AFC	00100	Space
AGC TIME CONSTANT:		
SLOW	01000	Line Feed
MEDIUM	00100	Space
FAST	01100	I
MODE:		
AM 2.5 KC	01000	Line Feed
AM 6 KC	00100	Space
CW 2.5 KC	01100	I
CW 6 KC	00010	Carriage Return
ISB	01010	R
FREQ:		
0	01000	Line Feed
1	00100	Space
2	01100	I
3	00010	Carriage Return
4	01010	R

TABLE 1-2. PUSHBUTTON CODES (Continued)

PUSHBUTTON (C-7775/UR, Figure 3-1)	5-BIT CODE, 12345	EQUIVALENT CCIT TTY CHARACTER
FREQ:		
5	00110	N
6	01110	C
7	00001	T
8	01001	L
9	00101	H
TUNE	10000	E
CLEAR	01111	V
FUNCTION:		
10 MC	11000	A
1 MC	10100	S
100 KC	11100	U
10 KC	10010	D
1 KC	11010	J
.1 KC	10110	F
MODE	11110	K
SYM/B2	10001	Z
B1	11001	W
A1	10101	Y
A2	11101	Q
FUNC	10011	B
EQUIPMENT SELECTION:		
A	10101	Y
B	10110	F
C	11010	J
D	11001	W
E	10011	B
1	00010	Carriage Return
2	01010	R
3	01100	I
4	01000	Line Feed

TABLE 1-2. PUSHBUTTON CODES (Continued)

PUSHBUTTON (C-7775/UR, Figure 3-1)	5-BIT CODE, 12345	EQUIVALENT CCIT TTY CHARACTER
EQUIPMENT SELECTION:		
5	00100	Space
6	01101	P
7	00101	H
8	00011	O
9/A	00111	M
10/B	01011	G

TABLE 1-3. READBACK CODES

CHARACTER RECEPTION ORDER	DISPLAY (ID-1600/UR, Figure 3-1)	INDICATION	CODE BITS	
			1	2345
1	Resets indicator for new cycle		1	0000
2	FREQUENCY/MEGACYCLES 10-mc digit	0		1111
		1		0111
		2		1011
		3		0011
	Receiver READY/TUNING/FAULT lamps	See Note *		
3	FREQUENCY/MEGACYCLES 1-mc digit	0		1111
		1		0111
		2		1011
		3		0011
		4		1101
		5		0101
		6		1001
		7		0001
		8		1110
		9		0110

*Readback for READY/TUNING/FAULT lamps is contained in bit #1 of codes #2 and #3 combined:

Code #2	Code #3	Lamp
1	0	READY
0	1	TUNING
1	1	FAULT

TABLE 1-3. READBACK CODES (Continued)

CHARACTER RECEPTION ORDER	DISPLAY (ID-1600/UR, Figure 3-1)	INDICATION	CODE BITS	
			1	2345
3 (cont)	Receiver READY/TUNING FAULT lamps	See Note *		
4	FREQUENCY/MEGACYCLES 100-kc digit	0 through 9	Same as for 1-mc digit (Character Reception Order 3)	
	EQUIPMENT SELECTED lamp	on	1	
		out	0	
5	FREQUENCY/MEGACYCLES 10-kc digit	0 through 9	Same as for 1-mc digit (Character Reception Order 3)	
	DECODER POWER lamp	on	1	
		out	0	
6	FREQUENCY/MEGACYCLES 1-kc digit	0 through 9	Same as for 1-mc digit (Character Reception Order 3)	
	NON AUTOMATIC lamp	on	1	
		out	0	
7	FREQUENCY/MEGACYCLES . 1-kc digit	0 through 9	Same as for 1-mc digit (Character Reception Order 3)	
	AFC ALARM lamp	on	1	
		out	0	
8	SYNTH/FUNCTION	on	1	1000
		out	0	1000
9	AFC/FUNCTION lamp	on	1	1000
		out	0	1000
10	Blank	none	0	0000

*Readback for READY/TUNING/FAULT lamps is contained in bit #1 of codes #2 and #3 combined:

Code #2	Code #3	Lamp
1	0	READY
0	1	TUNING
1	1	FAULT

TABLE 1-3. READBACK CODES (Continued)

CHARACTER RECEPTION ORDER	DISPLAY (ID-1600/UR, Figure 3-1)	INDICATION	CODE BITS	
			1	2345
11	MODE display	2.5 KC AM	0	1111
		6 KC AM	0	0111
		2.5 KC CW	0	1011
		6 KC CW	0	0011
		ISB	0	1101
12	AGC TIME CONSTANT display, SYM B2 and B1	SLOW and SLOW	0	1111
		SLOW and MED	0	1101
		SLOW and FAST	0	1110
		MED and SLOW	0	0111
		MED and MED	0	0101
		MED and FAST	0	0110
		FAST and SLOW	0	1011
		FAST and MED	0	1001
		FAST and FAST	0	1010
13	AGC TIME CONSTANT display, A2 and A1	SLOW and SLOW	0	1111
		SLOW and MED	0	1101
		SLOW and FAST	0	1110
		MED and SLOW	0	0111
		MED and MED	0	0101
		MED and FAST	0	0110
		FAST and SLOW	0	1011
		FAST and MED	0	1001
		FAST and FAST	0	1010
14, 15, 16	Blank	None	0	0000
	DISPLAY (SB-3230/UR, Figure 3-1)			
17	1-10 lamps (readback receiver identification)	1	0	1111
		2	0	0111
		3	0	1011

TABLE 1-3. READBACK CODES (Continued)

CHARACTER RECEPTION ORDER	DISPLAY (SB-3230/UR, Figure 3-1)	INDICATION	CODE BITS	
			1	2345
17 (cont)	1-10 lamps (readback receiver identification)	4	0	0011
		5	0	1101
		6	0	0101
		7	0	1001
		8	0	0001
		9	0	1110
		10	0	0110

1-5. EQUIPMENT SUPPLIED.

Table 1-4 lists all major components in Communications Control Console AN/URA-63 and includes accessories, special tools, and technical data supplied with each console.

1-6. EQUIPMENT AND PUBLICATIONS REQUIRED BUT NOT SUPPLIED.

A list of accessory and test equipment (and related publications) required but not supplied with the AN/URA-63 appears in table 1-5.

TABLE 1-4. EQUIPMENT SUPPLIED, AN/URA-63

QTY PER EQUIP.	NOMENCLATURE		UNIT NO.	OVERALL DIMENSIONS (IN.)			VOLUME (CU. FT)	WEIGHT (LB)
	NAME	DESIGNATION		HEIGHT	WIDTH	DEPTH		
1	Indicator Panel	SB-3230/UR	1	1.75	19	2	.04	2
1	Channel/ Frequency Indicator	ID-1600/UR	2	5.25	19	17	.98	37
1	Electronic Command Signal Programmer	C-7775/UR	3	7	19	15	1.15	26
1	Electrical Equipment Cabinet	CY-6538/URA-63	4	65	22	24	19.86	128
1	Maintenance Standards Book for AN/URA-63	NAVELEX 0967-385-1030	-	-	-	-	-	-
1	Operating Instruction Chart for AN/URA-63	NAVELEX 0967-385-1040	-	-	-	-	-	-
2	Technical Manual for AN/URA-63	NAVELEX 0967-385-1010	-	-	-	-	-	-
2	Operators Handbook	NAVELEX 0967-385-1020	-	-	-	-	-	-

TABLE 1-5. EQUIPMENT AND PUBLICATIONS REQUIRED BUT NOT SUPPLIED

QTY PER EQUIP.	NOMENCLATURE		REQUIRED USE	EQUIPMENT CHARACTERISTICS
	NAME	DESIGNATION		
1	Oscilloscope	AN/USM-281A	Trouble shooting and maintenance procedures	Horizontal amplifier: Response: dc to 5 mc Sensitivity: 0-1 v/div Maximum Input: 600 vdc Input impedance: 1 megohm, shunted by 30 pf (approx) Vertical amplifier, dual channel: Response (dc): dc to 50 mc Response (ac): 2 cps to 50 mc Rise time: 7 nsec Sensitivity: 0.005 volt/div Maximum input: ac; 600 v dc; greater than ±150 v Input impedance: 1 megohm, shunted by 25 pf (approx) Time base range: 0.05 usec/div to 2 sec/div
1	Frequency Counter	AN/USM-207	Trouble-shooting and maintenance procedure	Frequency range: dc to 50 mc Input: 0.1 vrms min 120 vrms max Input impedance: 1 megohm nominal shunted by 25 pf (approx)
1	Multimeter	AN/PSM-4C	Trouble-shooting and maintenance procedure	Voltage range: dc: 2.3 to 200 v ac: 0.1 to 250 v Circuit loading: dc: 20,000 ohms/volt ac: 5,000 ohms/volt Resistance measurements: 0 to 20 megohms
1	Teletypewriter	TT-176/UG or Equivalent	Trouble-shooting and maintenance procedure	Baud: 74.2
1	DC Loop Supply	Any capable of necessary characteristics		Current capabilities: 1 ma, 20 ma, 60 ma.
1	Instruction book for Oscilloscope AN/USM-281A	NAVSHIPS 0969-125-0110 (Vol. I) 0969-125-0120 (Vol. II)		
1	Instruction book for Frequency Counter AN/USM-207	NAVSHIPS 0969-028-4010 (Vol. I) 0969-028-4020 (Vol. II)		
1	Instruction book for Multimeter AN/PSM-4C	NAVSHIPS 0280-250-8004		

TABLE 1-5. EQUIPMENT AND PUBLICATIONS REQUIRED BUT NOT SUPPLIED (Continued)

QTY PER EQUIP.	NOMENCLATURE		REQUIRED USE	EQUIPMENT CHARACTERISTICS
	NAME	DESIGNATION		
1	Instruction book for Teletypewriter TT-176/UG	NAVSHIPS 0967-284-5010 (formerly NAVSHIPS 92361)		
1	Instructions for DC Loop Supply	Either: applicable NAVSHIPS publication, or applicable commercial manual.		

1-7. FACTORY OR FIELD CHANGES.

There are no factory or field changes in effect as of the issue date of this manual. Information pertinent to future changes will be available when a particular change is issued. Requests for updated information, if needed, should be addressed to the contractor.

1-8. RESHIPMENT DATA.

To prepare the AN/URA-63 for reshipment, proceed as follows:

a. Set all POWER switches to the OFF position, and disconnect AC input to console.

b. Remove the ID-1600/UR and the C-7775/UR from the console as indicated in steps (1) through (4).

(1) Remove front-panel mounting screws at each side.

(2) Slide unit out on tracks.

(3) Carefully disconnect all rear-panel cables.

(4) Disengage unit from track by depressing buttons on either side and pulling straight out.

WARNING

Remove ID-1600/UR from the console before removal of the C-7775/UR, to prevent a dangerous high center-of-gravity condition. Full weight of each unit must be supported upon removal from track.

c. Ensure that all cables are secured within console, and avoid sharp bends or snags.

d. Repack units in containers similar to those used to originally ship the equipment. Mark each container "FRAGILE-ELECTRONIC EQUIPMENT" on at least three sides.

SECTION 2

INSTALLATION

2-1. UNPACKING AND HANDLING.

The AN/URA-63 packing cases should be inspected for possible damage when they arrive at the operating site. With respect to damage to equipment for which the carrier is liable, the Technical Materiel Corporation will assist in describing methods of repair and the furnishings of replacement parts.

2-2. POWER REQUIREMENTS.

Each Console leaves the factory wired to operate from a 115-vac, 50/60-cps, single-phase power source. The Console can be rewired for operation from a 220-vac, 50/60 cps, single-phase source by changing transformer primary winding jumper leads in each rack modular unit. Refer to figure 2-1 for typical primary connections for 115- to 220-vac conversion. In units containing a blower, ensure that 115-vac is maintained across the blower as shown.

2-3. SITE SELECTION.

The Console may be located in any enclosure (room, deck, or van) with sufficient clearances as depicted in figure 2-2. Allow a minimum of 2 feet above and 1 foot behind the Console for adequate heat dissipation and to prevent back pressure in the cooling air exhaust stream. The Console is designed for fixed station, transportable, or ship installation. Remote readback into the Console is by means of conventional teletype linkage by a cable from the teletype loop current supply. The connector for this cable (INPUT J4) is located on the Channel/Frequency Indicator rear panel. The length of the cable should be consistent with the loop current supply, so as to prevent line drop (refer to paragraph 2-4b(3)(c)).

2-4. INSTALLATION REQUIREMENTS.

a. ASSEMBLY OF CONSOLE. - Install modular units and blank panels into the console as shown in figure 1-1. Connect modular unit power supply inputs to a-c power strip in Console as shown in figure 5-1. Refer to table 2-1 for summary list of installation materials. Modular units ID-1600/UR and C-7775/UR are slide mounted on tilt-lock drawer slides. The external part of the slide mount arrives pre-installed in the cabinet; the internal part arrives pre-installed on the modular unit. To install a unit, refer to figure 2-3 and proceed as follows:

(1) Pull the center section of the cabinet-mounted (external) portion of the slide mount out until it locks in an extended position.

(2) Position the unit-mounted (internal) portion of the slide mount in the tracks of the external portion and ease the modular unit into the cabinet until the release buttons engage the holes in the track.

(3) Depress the release buttons and slide the modular unit completely into the rack.

(4) Secure the modular unit front panel to the rack flange with machine screws and fiber washers supplied in shipment.

b. EXTERNAL WIRING CONNECTIONS. - All system wiring shall be connected at the rear panel

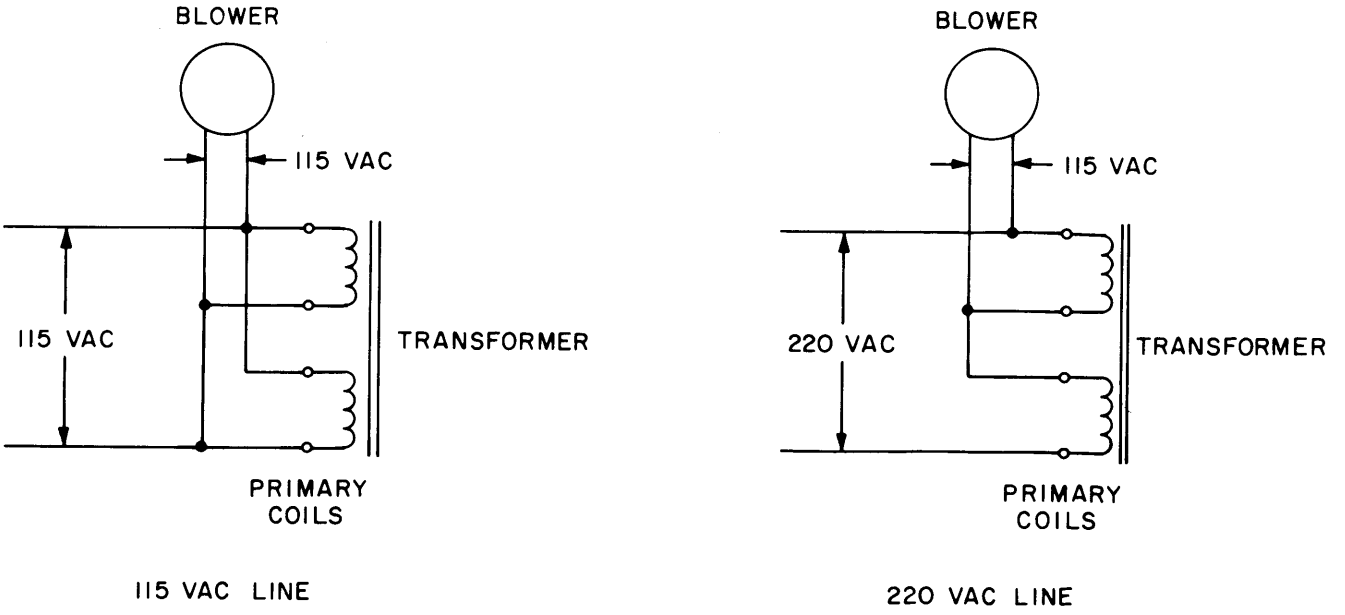
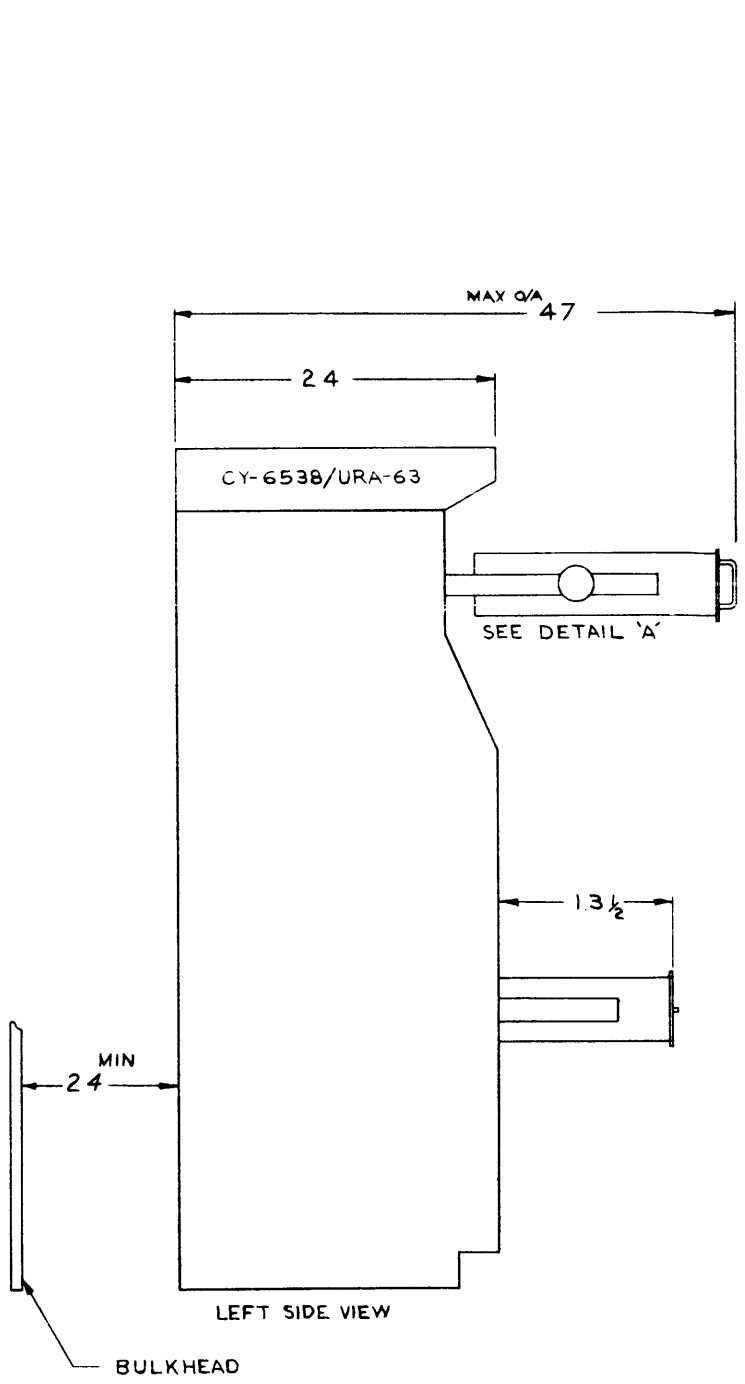
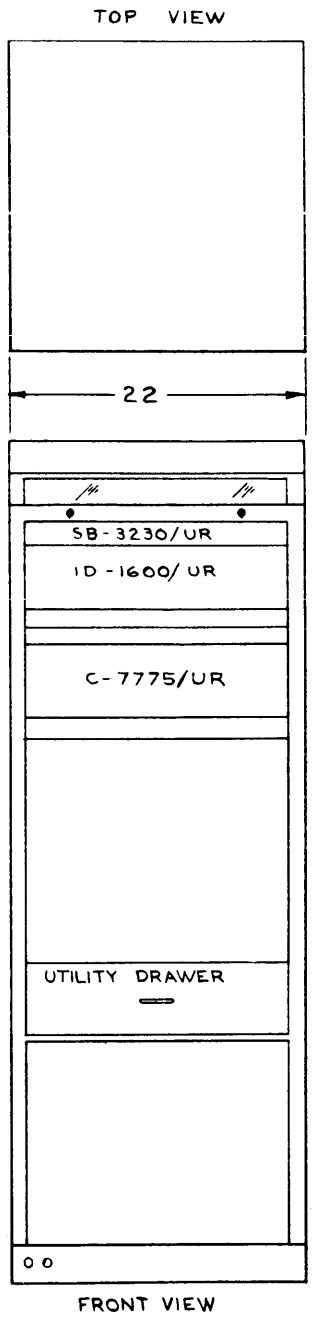
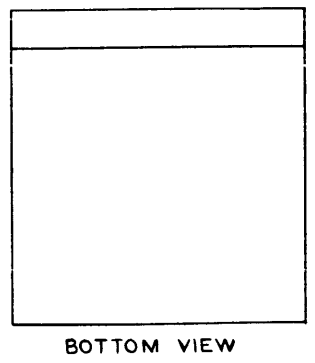


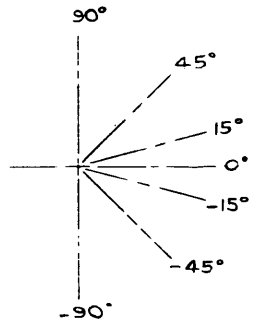
Figure 2-1. 115-220 Vac Conversion

NAVELEX 0967-385-1010

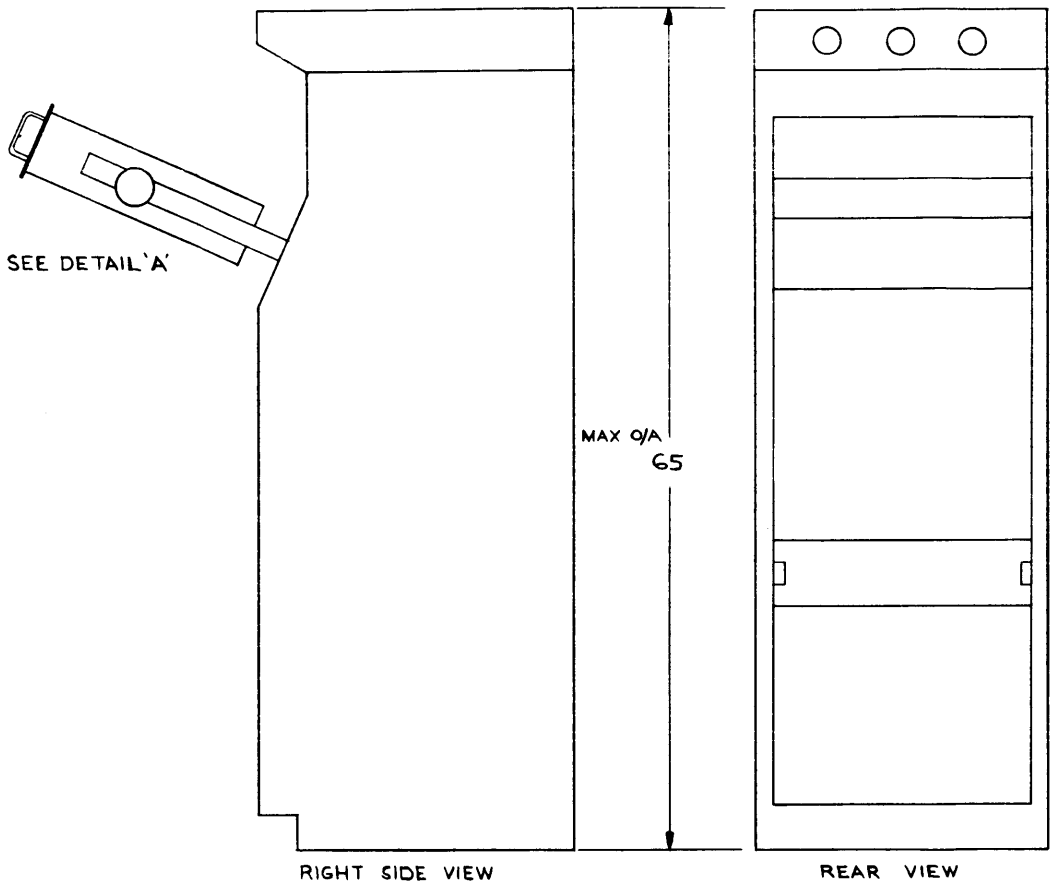








DETAIL 'A'
SERVICING POSITIONS
APPLICABLE ALL RACKS



UNIT DATA

POWER REQ'D	168 WATTS
HEAT DISSIPATION	573 BTU/HR
TEMP RANGE	0°-50°C
WEIGHT	193 LBS
CUBIC AREA	18 CU FT

CRATED DIMENSIONS

CONT NO.	L	W	H	CU AREA	WT
1	72	29	32 5/8	39.4 FT	435
2	36	26 3/4	34 3/4	19.4 FT	219

Figure 2-2. Outline and Dimensions, AN/URA-63 Cabinet

TABLE 2-1. SUMMARY LIST OF INSTALLATION MATERIALS

ITEM NUMBER	QUANTITY GF	QUANTITY CF	NOMENCLATURE	PART, TYPE OR MODEL NUMBER	REMARKS	SIZE LENGTH	SIZE HEIGHT	SIZE WIDTH
1		1	Panel, Indicator	SB-3230-UR	Unit 1	2	1.75	19
2		1	Indicator, Channel/Frequency	ID-1600/UR	Unit 2	17	5.25	19
3		1	Programmer, Electronic Command Signal	C-7775/UR	Unit 3	15	7	19
4		1	Cabinet, Electrical Equipment (& Cabling)	CY-6538/URA-63	Unit 4	24	65	22
5	1		Cable	TTRS-2 (1)	Programming Output			
6	1		Cable	TTRS-2 (1)	Readback Input			
7	1		Cable, AC Power	THFA-3	Power Input			
8		1	Grounding Strap	WL100-1 #10 AWG				
9		12	Screw, Machine	SCBP1032BN8	Unit MTG			
10		12	Washer, Fiber	WA101-11	Unit MTG			
11	1		Strap	WL100-7 #22 AWG	Readback Input (See 'TTY Loop' Chart)			
12		1	Connector, Plug	MS3106B20-27S	For Item 5 (Mates with 3J2)			
13		1	Connector, Plug	MS3106B20-27S	For Item 6 (Mates with 2J2)			

of Channel/Frequency Indicator ID-1600/UR and Electronic Command Signal Programmer C-7775/UR (see figure 5-1). For the AN/URR-63(V)2 receiver readback, the two loops will enter the cabinet and be connected to switch 4S2 (a double pole double throw switch). Switch 4S2 will allow the operator to select which half of the receiver (A or B) is to be displayed on the ID-1600/UR. Figure 2-4 contains wire-run information for constructing individual cables to each connector. Since the readback input requirements may vary, due to the quantity and types of the remote receivers, an analysis should be made as to necessary connections before proceeding to make up the cables. This analysis may be made from information contained in the following sub-paragraphs.

(1) PROGRAMMING OUTPUT. - The Console equipment may be arranged to control one single receiver, or an array of up to fifty single receivers; one dual-diversity receiver, or an array of up to twenty-five dual-diversity receivers. In all cases, one single teletype code channel output (DC LOOP, J2), from the C-7775/UR, controls all of the receivers in an arrangement. Single and dual-diversity receivers may be combined in an arrangement as long as receivers and receiver-halves do not exceed fifty when totaled up.

(2) READBACK INPUT. - Readback information from each receiver, however, comes back on a separate teletype channel. Cable connections to the ID-1600/UR may therefore vary in accordance with the particular arrangement. The ID-1600/UR contains a single input (INPUT J2) on its rear panel. Some varieties of receivers contain a device in which a readback is triggered by the EQUIPMENT SELECTION code push buttons on the C-7775/UR keyboard; in this case only one teletype channel is required for the readback input at the Console. For Receiving Sets AN/URR-63-(V)1 and 2, however, there are no triggering devices and the readback comes back on a separate teletype channel for each receiver or receiver "A" and "B" halves. For this purpose, a selector switch will be installed at the signal input to the Channel/Frequency Indicator (4S2).

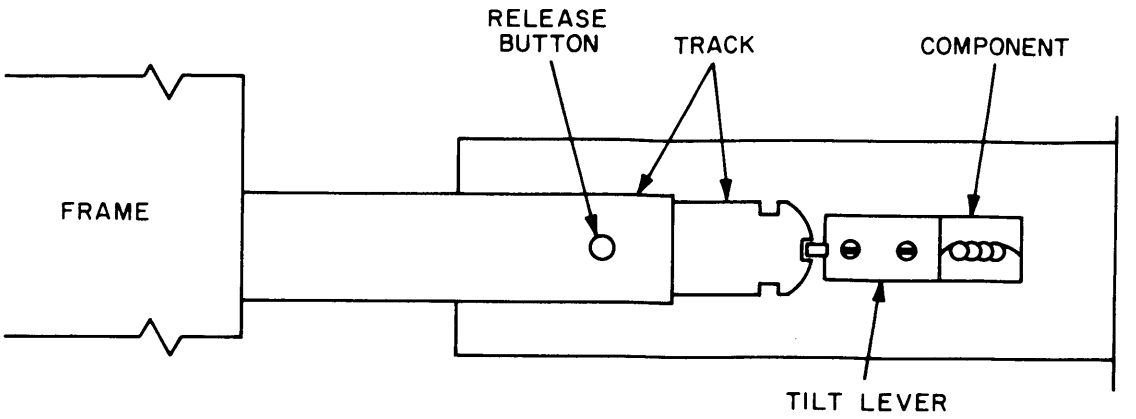


Figure 2-3. Slide Mount Details

(3) VARIATIONS IN TELETYPE LINKAGE EQUIPMENT.

(a) GENERAL. - Although the programming output and readback input circuits in the Console are designed to operate with 75 baud teletype linkages, these circuits are designed to adapt to a variety of baud ratings, current loops, and code levels in the teletype linkage equipment.

(b) BAUD RATING. - The baud rating at the readback input is determined by plug-in PC board A9 in the ID-1600/UR; the programming output is determined by plug-in PC board A3 in the C-7775/UR. In Communication Control Console AN/URA-63, these boards are designed for a 75-baud operation, although 45-baud PC boards are also available.

Note

Baud rating capacity of the Console is based on the clock timing circuit in the remote readback input. The timing circuit is designed to match pulse widths within each code.

(c) CURRENT LOOP. - In the readback input, the teletype equipment output current loop operates through isolation keyer PC board A2 in the Channel/Frequency Indicator. The keyer will operate from a 20 ma or 60 ma loop. When working from a 60 ma loop, resistor R5 on PC board A2 is bypassed by adding a strap around it at terminals provided on the board.

(d) CODE LEVELS. - Although the AN/URA-63 uses a 5- level code, programming code output and readback code input circuitry contains shift registers paced for 8-level teletype linkage equipment. No adjustments are necessary for the adaptation.

2-5. CABLE ASSEMBLIES.

The programming output cable and the readback input cable should be wired in accordance with wire-run information in table 2-2. Refer to paragraph 2-4b(2) if more than one receiver is to be readback.

2-6. INSPECTION AND ADJUSTMENT.

a. ENERGIZING EQUIPMENT. - Ensure that all connections have been properly made and that the AN/URA-63 is receiving proper supply voltage, and then proceed as follows:

(1) Set POWER switch on ID-1600/UR to ON. Blower should start, and digital readout should illuminate. If Console is connected to a receiver that is properly set for remote operation, and if the receiver is energized, a readback of receiver status may appear. *

(2) Set POWER switch on C-7775/UR to ON. Power indicator should illuminate. If Console is connected to an energized receiver that is properly set for remote operation, it should be possible to remotely tune the receiver. If readout ID-1600/UR is operative, it will display results of the tuning, when the receiver is properly addressed. Refer to Section 3, Operation, for programming instructions.

Note

If blower did not start, nor indicators illuminated, in the above steps, recheck all ac power input wiring. Ensure that: (a) Console is receiving supply voltage (check main breakers at site); (b) Each unit is properly wired for the ac input voltage being used (if a wiring change was made, be certain that all units have been similarly rewired); and (c) All fuses are intact. (Check indicator/holders. If any one is illuminated, twist ccw, pull straight out, replace fuse cartridge, reinsert, and twist cw to lock.) If fuses continue to open-circuit after replacement do not replace further. A trouble-shooting procedure is indicated for the ac power input section of the faulty unit (the power supply sections occurring after the input contain a short-proof circuit, and would therefore not cause an open-circuit).

*Due to starting transients, the readback may not be accurate; also, the ID-1600/UR may begin a display in the midst of a readback cycle, which would also produce a false readout. This condition will correct itself within six seconds. If no readback, check that Isolation Keyer 2A1 is receiving +6 vdc at board pins 12 (hot) and 15 (gnd). This corresponds to input connector 2J2 pins E and D respectively. See figure 2-4.

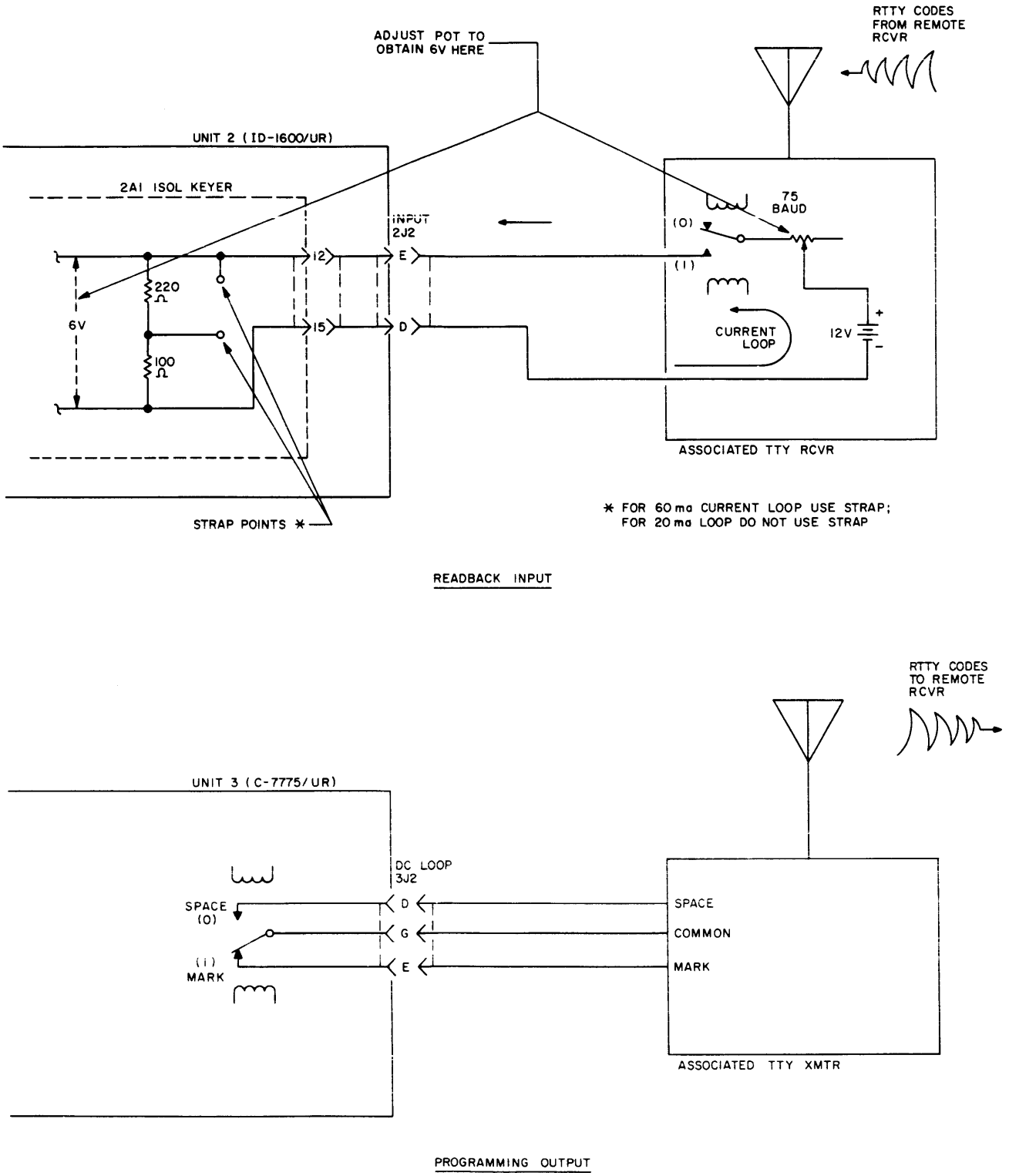


Figure 2-4. External Wiring Connections

TABLE 2-2. WIRE-RUN LIST, EXTERNAL CABLING

NAVY CABLE DESIGNATION	NO. OF ACTIVE CONDS	FROM	TERMINAL BOARD, PLUG OR JACK	TERMINAL DESIGNATION OR PIN	TO	FUNCTION
TTRS-2	4	Unit 3, Rear Panel	3J2	D F G H E	TTY XMTR	Programming output: USE ONE { LO LEVEL NO 20mA / HI LEVEL NO 60mA } COMMON USE ONE { HI LEVEL NC60mA / LO LEVEL NC 20mA }
TTRS-2	4	Unit 4	4S2	1 4 3 6	TTY RCVR	Readback Input A + - Readback Input B + -
THFA-3	2	Power Source			Power Strip	AC POWER INPUT

b. CHECKOUT PROCEDURE. - Checkout procedure will ascertain correct transmissions and reception of tuning and readback codes by the AN/URA-63. For proper checkout, a TT-176/UG or similar 5-level, 74.2 band teletypewriter will be required, as well as a suitable dc loop supply. Checkout will proceed as follows:

(1) ID-1600/UR FREQUENCY AND PROJECTION READOUTS. - Connect teletypewriter keyboard output to input of ID-1600/UR, in series with "send loop" supply, as depicted in figure 2-4. (Keyboard output should be substituted for the TTY receiver and adjusted and strapped at 2A1 as shown.) Energize both ID-1600 and teletypewriter, and perform in order, the following (characters shown are CCIT teletype characters):

(a) Type out:
E, followed by 16 Vs.
ID-1600 should read (top row left-to-right; temporarily ignore Receiver Status indicator lamps):
00.0000, AM 2.5 kc, SLOW/SLOW, SLOW/SLOW.
SB-3230 should read: 1.

(b) Type out:
EVMVMVMVVVMPMVVVM
ID-1600 should read:
01.0101, AM 6 kc, SLOW/MED, MED/SLOW.
SB-3230 should read: 2.

(c) Type out:
EMGMGMGVVVGCHVVVG
ID-1600 should read:
12.1212, CW 2.5 kc, SLOW/FAST, MED/MED.
SB-3230 should read: 3.

(d) Type out:
EGOGOGOVVVOMNVVVO
ID-1600 should read:
23.2323, CW 6 kc, MED/SLOW, MED/FAST.
SB-3230 should read: 4.

(e) Type out:
EOPOPOPVVVPHCVVVP
ID-1600 should read:
34.3434, ISB, MED/MED, SLOW/FAST.
SB-3230 should read: 5.

(f) Type out:
EPHPHPHPHVVVVNRVVVH
ID-1600 should read:
45.4545, AM 2.5 kc, MED/FAST, FAST/FAST.
SB-3230 should read: 6.

(g) Type out:
EHLHLHLVVVVGPVVVL
ID-1600 should read:
56.5656, AM 2.5 kc, FAST/SLOW, SLOW/MED.
SB-3230 should read: 7.

(h) Type out:
ELTLTLTVVVVLGVVVT
ID-1600 should read:
67.6767, AM 2.5 kc, FAST/MED, FAST/SLOW.
SB-3230 should read: 8.

(i) Type out:
ETCTCTCVVVVRLVVVC
ID-1600 should read:
78.7878, AM 2.5 kc, FAST/FAST, FAST/MED.
SB-3230 should read: 9.

(j) Type out:
ECNCNCNVVVVVVVVVN
ID-1600 should read:
89.8989, AM 2.5 kc, SLOW/SLOW, SLOW/SLOW.
SB-3230 should read: 10.

(k) Type out:
ENVNVNV
ID-1600 should read:
90.9090; remainder of display same as (j).

(2) ID-1600/UR RECEIVER STATUS INDICATOR LAMPS. - Test setup is the same as that used in (1). Disregard all projection readouts as well as SB-3230 display; observe only frequency readout and Receiver Status lamps. Proceed as follows (only in order listed below):

(a) Type out:
E followed by 16 Vs.
ID-1600:
00.0000, DECODER POWER lit (will flicker off, and return on, in subsequent steps).

(b) Type out:
E
ID-1600 should read:
00.0000, DECODER POWER lit.

(c) Type out:
B
ID-1600 should read:
30.0000, DECODER POWER, TUNING lit.

(d) Type out:
L
ID-1600 should read:
36.0000, DECODER POWER, TUNING lit.

(e) Type out:
Y
ID-1600 should read:
36.5000, DECODER POWER, TUNING, EQUIPMENT SELECTED lit.

(f) Type out:
Y
ID-1600 should read:
36.5500, DECODER POWER (will not flicker again, until step (1)), TUNING, EQUIPMENT SELECTED lit.

(g) Type out:
Y
ID-1600 should read:
36.5550, DECODER POWER, TUNING, EQUIPMENT SELECTED, NON-AUTOMATIC lit.

(h) Type out:
Y
ID-1600 should read:
36.5555, DECODER POWER, TUNING, EQUIPMENT SELECTED, NON-AUTOMATIC, AFC ALARM lit.

(i) Type out:
A
ID-1600 should read:
36.5555, DECODER POWER, TUNING, EQUIPMENT SELECTED, NON-AUTOMATIC, AFC ALARM, and SYNTH lit.

(j) Type out:
S
ID-1600 should read:
36.5555, DECODER POWER, TUNING, EQUIPMENT SELECTED, NON-AUTOMATIC, AFC ALARM, SYNTH, AFC lit.

(k) Type out:
VVVVVVVVELQ
ID-1600 should read:
TUNING lamp extinguishes and READY lamp illuminates; otherwise, same as step (j).

(l) Type out:
14 Vs, followed by an E
ID-1600 should read:
34.0000, READY, DECODER POWER.
(will again flicker).

(m) Type out:
B
ID-1600 should read:
34.0000, FAULT, DECODER POWER.

Note

The ID-1600/UR is considered fully operational, if it has responded as indicated in checkout procedures (1) and (2).

(3) C-7775/UR PUSHBUTTON CODES. - To determine operational correctness of Programmer C-7775/UR proceed as follows:

(a) Connect, in series, Programmer C-7775/UR, teletypewriter "receive"loop, and receive loop supply. Programmer output appears at connector 3J2 pin D (space), G (common), and E (mark).

(b) Refer to table 1-2 (Pushbutton Codes), depress the programmer button indicated in column 1 of the table, and observe the teleprinter's response. The printer should execute the CCIT character indicated in column 3. Thus, if the 10 mc button is depressed on the FUNCTION row, the printer should respond by printing the letter A.

Note

If a correct response is obtained for each button indicated in the table, the programmer is considered operational. Disregard blank buttons on the programmer.

(c) Disconnect temporary checkout connections and restore normal operational connections.

SECTION 4

TROUBLE SHOOTING

4-1. LOGICAL TROUBLE SHOOTING PROCEDURE.

a. INTRODUCTION. - The procedure described in this section is aimed at directing the trouble shooter to the faulty component, connection, or wire by logical choice and in as few steps as possible. The basis for the steps is the structure of the Console. The Console is divided into three modular units, each unit having a unique and independent function (i. e., programming or readback). The ID-1600/UR and C-7775/UR modular units are further subdivided into removable plug-in PC (printed circuit) boards and other subassemblies. In the trouble shooting procedure, a faulty subassembly can be removed and replaced quickly, placing the AN/URA-63 back in operation; trouble shooting (and repair) of the removed subassembly can then be continued at a different time or locality, if necessary. In trouble shooting the AN/URA-63, there are five basic steps to be taken; these are:

(1) Symptom recognition.
(2) Symptom elaboration.
(3) Determining the faulty modular unit.
(4) Localizing the faulty subassembly within the unit.
(5) Localizing the faulty component within the subassembly.

b. SYMPTOM RECOGNITION. - At the first sign of trouble, it is important to determine whether or not it is the AN/URA-63 that is causing the trouble or one of the associated equipments (i. e. : remote receiver, teletype linkage, readback transmitter in the remote receiver, etc.).

c. SYMPTOM ELABORATION. - After it has been determined that the AN/URA-63 is at fault, the symptom should be examined more closely. Using the keyboard in the Programmer, and referring to the operating procedures in Section 3, experiment with all of the buttons in order to define which area is giving trouble.

d. DETERMINING THE FAULTY MODULAR UNIT. - When the area of the trouble has been defined, refer to table 4-1, Trouble Shooting Chart. This chart will serve as an aid in determining whether it is a programming or readback problem and in identifying the faulty modular unit. If necessary, reference may also be made to paragraph 4-2 for primary test input and output values.

TABLE 4-1. TROUBLE SHOOTING CHART, AN/URA-63

SYMPTOM	FUNCTIONAL SECTION INDICATED
DECODER POWER lamp is out but new programming of receiver fails to bring a change on display of ID-1600/UR panel.	Readback (ID-1600/UR)
Lamps 1 through 10 on SB-3230/UR panel extinguished.	Readback (ID-1600/UR)
One lamp in the 10 lamp display on SB-3230/UR panel fails to light.	Readback (SB-3230/UR)
ID-1600/UR EQUIPMENT SELECTED lamp fails to light after C-7775/UR EQUIPMENT SELECTION buttons are pushed.	Programming (C-7775/UR)
ID-1600/UR FAULT lamp does not light, although FREQUENCY/ MEGACYCLES readback cannot be made to match programmed figures.	Readback (ID-1600/UR)
A particular pushbutton on the C-7775/UR fails to bring results as evidenced in the readback.	Programming (C-7775/UR)
ID-1600/UR EQUIPMENT SELECTED lamp lights but C-7775/UR TUNE pushbutton fails to precipitate tuning in receiver as evidenced in readback display.	Programming (C-7775/UR)

e. LOCALIZING THE FAULTY SUBASSEMBLY WITHIN THE MODULAR UNIT. - When the faulty modular unit has been discovered, it may be left in the Console for purposes of system trouble shooting or it may be removed for bench test trouble shooting. In either case, reference to either the programming functional section description or the readback functional section description in paragraph 4-2 and their accompanying paragraphs on functional section test data should reveal the faulty subassembly, PC board, or wiring connection area. Subassemblies may be located by referring to major component location diagrams for each modular unit in Section 5. A quick short-cut can be performed in this step by using spare plug-in subassemblies for a substitution check to reveal the faulty subassembly.

f. LOCALIZING THE FAULTY COMPONENT WITHIN THE SUBASSEMBLY OR AREA. - When the faulty subassembly has been discovered, it is generally expeditious to replace it from the spares supply. Further trouble shooting of the subassembly may then be performed in a modular unit at a different site or time. For this latter purpose, the technician may refer to paragraph 4-3, Subassembly Description. The text in subparagraphs of 4-3 is divided into subassemblies and because of the complex and interrelated nature of the subassemblies, are presented in their functional order. The text refers to subassembly schematics in Section 5. Before starting subassembly trouble shooting, the technician should check the Notes column opposite the subassembly listing in Section 6, Parts List. Some subassemblies have been categorized by the provisioning agency as non-reparable from a practical or costwise point of view. In addition, some subassemblies are recommended to be returned to the factory for repair. In both cases, there should be spare subassemblies available for replacement, eliminating the necessity for any further trouble shooting procedures.

4-2. FUNCTIONAL SECTION DESCRIPTIONS (See Figure 4-1).

a. INTRODUCTION. - The following text is a description of the functioning of major plug-in assemblies and is divided into the programming and readback functions of the AN/URA-63. The programming function is entirely contained in Electronic Command Signal Programmer C-7775/UR. The readback function is contained in Channel/Frequency Indicator ID-1600/UR and Indicator Panel SB-3230/UR. All circuitry (with the exception of the power supplies) is in encapsulated binary logic networks with binary d-c inputs and outputs at each network. Therefore the functional theory in this paragraph and the detailed theory in paragraph 4-3 is referenced to accompanying timing charts. These charts more precisely describe the operation throughout the equipment and shall be used for the actual testing of the equipment. Refer to paragraph 4-2e for procedure in reading and using the timing charts.

b. TEST EQUIPMENT REQUIRED. - A list of test equipment necessary to trouble shoot and maintain the AN/URA-63 appears in table 1-5, Equipment and Publications Required but not Supplied.

c. PROGRAMMING (See Figures 4-2 and 5-27). -

(1) FUNCTIONAL DESCRIPTION. - The C-7775/UR is primarily a teletype code generator. Components of the generator are keyboard assembly A6, code register A5, shift register A3, gating circuit A4 and output keyer A2. Power supply A1 furnishes the logic voltages for all the components.

Keyboard assembly A6 consists of three rows of pushbuttons all with a common mechanical linkage. The linkage is arranged so as to hold a pushed-in button down until the next button is pushed in. The two exceptions to this are the CLEAR button (A6S13) and the TUNE button (A6S14). Although they also release previously pushed-in buttons, they are momentary-contact types and pop up (break contact) when released. Each button forms a switch closure with ground and the ground is extended to code register A5.

When a ground reaches a particular input on code register A5, a 5-bit code is setup (refer to table 1-2). The bits of this code appear simultaneously (parallel bits) at pins 15, 3, Y, B and F of A5. These bits are then brought over to gating circuit A4. The arrival of the bits of each code at gating circuit A4 generates a pulse to pin C of shift register A3, starting a clock (timing generator) in A3. The clock energizes a shift register in A3 and this proceeds to shift each bit of the code (one-by-one) over to output keyer A2. The code appears at the output of A2 in the form of contact keying from a polarized relay. Depending on the TTY equipment to be run, either a high level or a low level output may be used; the high level output offers more resistance in the line (refer to paragraph 2-b(1)).

Shift register A3 shifts ten times. The first shift creates the start pulse, the next five shifts move the bits out to the keyer, and the remaining four shifts give the C-7775/UR the ability to work with 7- or 8-level teletype sending equipment (rather than 5-level) if 5-level equipment is not available. The shift rate is 75 baud. At the end of the cycle, the last shift turns off the clock. When the next button is pushed and the next code arrives at A4, the energizing pulse from A4 restarts the clock and the cycle is repeated.

(2) TEST DATA. - To test subassembly inputs and outputs of the programming section, see figure 4-1 and measure at PC board pin numbers. Overall input-versus-output may be tested first by using a teletype receiver (if available) at the output (see figure 2-4 for polarity) and pushing buttons on the keyboard. For this purpose, table 1-2 (Pushbutton Codes) includes an "equivalent CCIT TTY character" column; these characters should appear in the readout.

d. READBACK (See Figures 4-3, 5-2 and 5-4).

(1) FUNCTIONAL DESCRIPTION. - The ID-1600/UR is the display unit for a continuous cycling of teletype readback codes from the remote receiver (refer to table 1-3). These codes represent specific receiver control positions and, in general, the receiver's status in a remote tuning operation. The last code to be received in each cycle is a receiver identification code. This represents a 1 through 10 number, signifying which receiver in a block of ten is represented in the readout. The signal for this is forwarded from the ID-1600/UR unit to one of the ten

lamps on Indicator Panel SB-3230/UR, via the connection of ID-1600/UR receptacle J1 and SB-3230/UR plug P1.

As the serial teletype pulses of each code enter the ID-1600/UR, they are converted into parallel pulses. The serial pulses (see figure 5-4) enter the ID-1600/UR at receptacle J2 and pins 12 and 15 of isolation keyer A2. Pulses are from a standard keyed teletype current loop and include a start pulse at the beginning and a stop pulse at the end. A keyer at the output of A2 keys a -12 volt logic voltage at the timing circuit A9 input. Timing circuit A9 converts these serial pulses into five parallel bit pulses (for each code) and routes them to timing circuit A8. Timing circuit A8 places bit 1 information on lamp driver A3 and bits 2 through 5 information simultaneously on frequency gating circuits A5 and A4 and position driver cards A16, A15, A14 and A1. Readout will not occur from a particular driver or gating circuit, however, until a gating pulse is received from the shift register.

The shift register (composed of PC boards A7 and A6) produces sixteen gating pulses (one for each code). Gating outputs are connected to the various drivers and gating circuits in order to read out each code in a certain order; which is the predetermined order that the cycle of codes arrives from the remote receiver readback transmitter. In this manner the code that is intended to drive a particular display is read out on that display. A cycle of gating pulses appears in the following order:

1. 10 MC
2. 1 MC
3. 100 KC
4. 10 KC
5. 1 KC
6. 0.1 KC
7. Function 1
8. Function 2
9. Function 3
10. Function 4
11. Function 5
12. Function 6
13. Function 7
14. Function 8
15. Function 9
16. Function 10

The FREQUENCY/MEGACYCLES gating pulses are for reading out the six codes for the six digits on the front panel display. Functions 1 through 10 gating pulses are for reading out a variety of codes and these vary from receiver to receiver. Specifically, for the ID-1600/UR, function 4, 5, 6, and 10 gating pulses are used; function 1, 2, 3, 7, 8 and 9 pulses are not used. Chassis wiring is of universal design and includes receptacles and sockets for the full complement of drivers and display units for all ten readout functions. At the beginning of the cycle, A7 produces eight shifts (or gating pulses) and triggers shift register A6. Shift register A6 then produces eight additional shifts making the total sixteen.

There are three types of display on the ID-1600/UR front panel: (a) a digital readout display, (b) a lamp display, and (c) a projection readout display. The six digital readout (FREQUENCY/MEGACYCLES) displays (DS10, 11, 13, 14, 15 and 16) are driven by six BCD* decoders: ZX10, 11, 13, 14, 15 and 16. The decoders, in turn, receive a BCD input from the frequency gating circuits, A5 and A4. The resulting output from a decoder is one ground signal; this ground forms a return for +200 volts through a 0 through 9 digit-shaped filament in the indicator. Lamp DS12 forms the decimal point in this display and is on all the time. The nine-lamp display, to the right of the digital readout, is for a variety of information and panel lettering varies on different models. The specific panel lettering for the ID-1600/UR is shown in figure 5-4. Each lamp is individually controlled by a ground signal from lamp driver A3. Directly below the digital readout, on the front panel, is the projection readout display group. This group contains spaces (and sockets) for nine indicator units, DS17 through DS25. Each indicator unit is driven by a PC board driver (A11 through A19). Drivers and projection readout pairs may be a 12-position type for a receiver control of up to 12 positions, or a dual 4-position type for two receiver controls of up to 4 positions each. Panel lettering will also vary from model to model. Specifically, for the ID-1600/UR, three of the nine spaces are utilized; these are:

Function	Posn Type	Driver	Readout Unit	Panel Marking
4	12-posn	A16	DS20	MODE
5	dual-4	A15	DS21	AGC TIME CONSTANT SYM/B2-B1
6	dual-4	A14	DS22	AGC TIME CONSTANT A2-A1

Drivers A11, 12, 13, 17, 18, and 19 and readout indicators DS17, 18, 19, 23, 24, and 25 are not included in the make-up of the ID-1600/UR, although sockets are present in the universal wiring. Each driver receives a code and (upon the receipt of its gating pulse) presents one ground signal to its indicator. The indicator contains a grid of lamps, one for each input. The lamp receiving the ground lights and, via an individual projection lens and film in front of it, casts the image of the film onto the indicator projection screen.

The final code to arrive in the cycle (refer to table 1-3) is for receiver identification. This code, representing a 1 through 10 figure, is gated from driver A1 (in the ID-1600/UR configuration) to produce a ground from one of its outputs to one of the ten lamps in Indicator Panel SB-3230/UR. Information in one code is often for more than one display. The digital readouts always use bits 2 through 5. Bit 1 of the first six codes, however, drives other displays. Reference to table 1-3 will show these specific cases for the ID-1600/UR configuration. It may be seen, as in the case of the 10 mc and 1 mc code transmissions, that significant information is contained in the polarity relationship of bit 1 in two successive codes. In the case of codes intended for dual 4- position indicators (the AGC TIME CONSTANT displays), one code contains information for two receiver controls. A two-bit code for each control depicts one of four possible positions for the control. In the SYM/B2-B1 display,

*binary coded decimal

bits 2 and 3 represent the SYM/B2 control and bits 4 and 5 represent the B1 control. In the same manner, in the A2-A1 display, bits 2 and 3 represent A2 and bits 4 and 5 represent A1.

The "E" teletype character (refer to table 1-3) is the first to arrive in each readback cycle and functions to reset ID-1600/UR circuitry for the new cycle. The E code (10000) causes an "E" pulse to issue from pin 2 of A8 to pin R of shift-register A7, setting it for the new cycle. The bit shift-register in timing circuit A9 is so arranged as to allow ten shifts, in a time interval of 135* milliseconds, for the passage of each code. This corresponds with the time required for a standard 8-level transmission and adapts the ID-1600/UR to operate from a 7-level or 8-level teletype linkage, if 5-level is not available. In all cases, pulse widths, in the shift register, are 13.5 milliseconds for receiving a 75-baud rate.

(2) TEST DATA. - To test subassembly inputs and outputs of the readback section, see figure 4-3 and measure at PC board pin numbers. The timing chart is the normal pattern for a specific test code input; this test input can be from a specific remote receiver control setup or from a teletype sender attached locally to receptacle J2 (see figure 2-4 for polarity). For the latter purpose, specific CCIT teletype keyboard characters are included on the timing chart.

e. USAGE OF TIMING CHARTS. - Timing charts, figures 4-2 through 4-3, are categorized by Console functional sections involving binary logic and subdivided further into phases and modes of these sections. Each line represents a test point time variance between two voltage values and all lines are plotted against a common time base for comparison. Test points are arranged from top to bottom in normal order of checking (input to output) a functional section, or subdivision thereof.

Using time bases A and B of the oscilloscope, check testpoints in pairs (the test point and the one directly below it on the chart) at coinciding pulse edges (voltage changes). This comparison check will reveal, by reference to the PC board logic schematic in Section 5, the logic network/component to be replaced. To make a measurement, set the oscilloscope for an internal triggering mode; with a negative triggering slope and level for a negative-going change and a positive triggering slope and level for a positive-going change. The exact shape of the pulse edge is not an important factor in trouble shooting the binary logic sections. Very often, different attenuator lines at the input of the oscilloscope will produce pulse shape distortions that are not present in the equipment being tested. The critical fact is whether or not the expected voltage changes occur in the polarities and coincidences as indicated on a common time base.

Due to the digital nature of the equipment, timing charts are provided in lieu of servicing block diagrams in order to present more graphically the operating parameters of the equipment. These timing charts (figures 4-2 and 4-3) provide the input and output waveform information for the subassemblies. They should be used with figures 5-4 and 5-27 to localize the faulty subassembly. The timing charts also provide waveform information within the subassemblies which, when used with the respective figure for a particular subassembly, aids in localizing faults within the subassembly.

*220 and 22 milliseconds for 60 WPM equipment.

4-3. SUBASSEMBLY DESCRIPTION.

a. INTRODUCTION. The following information is to be used in trouble shooting to locate the faulty component or area within a subassembly. Refer also to NAVSHIPS 0967-000-0120 for information pertinent to standard circuits.

b. UNIT 1 (SB-3230/UR) (See figure 5-2). - Unit 1 indicates which remote receiver in a block of up to 10 units is reading back its current status. Unit 1 receives: -12 vdc (pin P) and a ground provided by 2A1 at a particular pin (pins F, D, J, G, L, S, E, R, H, K), and produces a visual indication of the active receiver by means of 10 numbered lamps (1 through 10), one of which will be illuminated. The unit consists of 10 pilot lamps mounted behind small numbered panels, all mounted on a 19-inch wide main panel. Connections to these lamps are made through plug P1, at the end of the interconnecting cable between Unit 1 and Unit 2. The -12 vdc input enters Unit 1 at pin P and is routed to one side of all 10 lamps; however, only one of these lamps will be returned to ground through 2A1 at any one time. The particular lamp to be illuminated will depend on the four-bit receiver identification code (last code in the readback sequence) applied to the input of 2A1. For further information, refer to paragraphs 4-3i,j, and k.

c. UNIT 2 (ID-1600/UR) 2A10 POWER SUPPLY BOARD (See figure 5-23). - Power supply board 2A10 contains three sections, providing +12 volts regulated, -12 volts regulated, and +200 volts zener-regulated. Input to each section is supplied by a separate secondary winding of power transformer 2T1. Because both 12-volt sections are quite similar in operation, only the +12 vdc and +200 vdc sections need be fully explained; the difference between the +12 vdc and -12 vdc will also be noted. Unless preceded by the unit number, all reference designations refer to components physically mounted on A10; thus, C7 in the following explanation refers to 2A10C7; 2C7 would refer to a component mounted external to 2A10.

Incoming ac (pins 20 and 21) is rectified by full-wave bridge rectifier CR2, and passes through a surge limiter consisting of R16 and R17. The resultant pulsating dc is applied to pin 3 of Z2 which is an integrated voltage regulator, incorporating current limiting and short-circuit overload protection. Essentially, Z2 functions as an operational amplifier with heavy feedback. An output of Z2 is applied to the base of driver Q4. Driver Q4, along with R11, forms a divider-bias network for series-pass transistor Q3, which performs the actual regulation. The collector-emitter path of Q3 is in series with the filtered output of CR2 (filtering is accomplished external to 2A10 by capacitor 2C2, connected between board pin V and ground); Q3 thus acts as a series resistance, varied by Z2, via Q4. Therefore, voltage output is ultimately

regulated by Z2. To regulate properly, however, Z2 must have an error input; this input is obtained by sampling the output voltage at the junction of the voltage divider formed by R9 and R10. The error sample is applied as feedback input to terminal 6 of Z2. Within Z2, the error input is compared with an internal voltage reference standard in what amounts to a differential amplifier; output of this amplifier is applied to the base of Q4. Capacitor C4, connected between terminals 6 and 7 of Z2 is part of an internal frequency compensation network, to prevent oscillation at high frequencies and/or transient "ringing". Capacitor C2 bypasses stray pickup, and resistor R15 is an output bleeder.

Current limiting is accomplished by Z2 in conjunction with resistors R12, R13, and R14. Limiting is of the "switchback" type, i. e. when a heavy current overload occurs, the switchback limiter reduces current flow to a relatively small fraction of maximum output, instead of simply limiting current flow to the maximum design value until the overload is removed. Limiter operation is as follows: Output current creates a voltage drop across R14, which would appear between Z2 terminals 1 and 8; however, the divider composed of R12 and R13 causes another voltage drop; this drop bucks out the drop across R14. Consider the case of a short circuit at the output; R12 and R13 are effectively in parallel across the output, therefore, the voltage across the combination approaches zero and the bucking voltage is no longer generated. The heavy current through R14 causes a relatively large drop to appear between Z2 terminals 1 and 8; these terminals become the current-limiting input terminals. Voltage regulator Z2 immediately reacts by reducing forward bias on Q3 until output current returns to a safe predetermined value (in this case, about 0. 5 amp). The combination of R12 and R13 also provides a pre-load on the output of about 20 ma, so the regulator will always operate into a load. Terminal 4 of Z2 is ground input for the IC.

The -12-volt section of 2A10 functions in an identical manner to the +12-volt section, with the following exceptions: the -12 vdc series-pass transistor 2Q1 is mounted external to the board at pins L (emitter), 8 (collector), and D (base); full-wave bridge rectifier 2CR1 is also mounted external to 2A10, at pins 8 (+), and 5 (-). The surge limiter resistors are not used in this section; instead, a capacitor across 2CR1 provides a very low initial surge impedance, thus shunting any initial transients away from current-sensitive components on 2A10. Due to the polarity inversion, the current limiter bucking divider is connected between emitter of Q1 and the -12-volt line.

The +200 vdc section of 2A10 is comprised of CR1, R8, 2CR2, 2R1, and 2C3. A potential of 280 vac from a winding of 2T1 enters 2A10 at pins B and 3, and is rectified by CR1. The pulsating dc is then fed out of 2A10 (pins C, 2); the positive lead (pin C) passes the voltage through 2T1, which, along with 2C3 across the output forms a simple filter. Zener diode 2CR2, also across the output, maintains the output voltage at +200 vdc, and resistor R8 on 2A10 is a bleeder. The +200 vdc output is taken between pin 4 (hot) and pin N (return not grounded).

d. UNIT 2; 2A2 ISOLATION KEYER (See figure 5-11). - Isolation Keyer 2A2 converts current-keyed TTY input to standardized logic levels for MARK and SPACE, for use by the entire unit. The 2A2 receives 20 vac (pins X, W), -12 vdc (pin 4), and serial TTY current-keyed input (pin 12, +; pin 15, -) and produces serial TTY code logic levels of -12 vdc MARK and 0 vdc SPACE (pin B). The keyer consists of a mercury-wetted polar relay, a rectifier-filter to supply coil voltage for the relay, and a transistor keying circuit. A potential of 20 vac from one of the secondary windings of 2T1 enters 2A2 at pins X and W, and is rectified by CR4 and filtered by network R2, C2, C3. The resultant dc is applied to the SPACE coil of K1 through bias resistor R4, and returned to the common leg of the circuit. Resistor R4 is adjusted to hold K1 in a SPACE condition, with no TTY current input. TTY current is drawn through input loop R5, R6 (R6 bypassed for 60 ma operation) from PC board pins 12 (loop +) and 15 (loop -). The voltage developed across the resistors places approximately +6 vdc, base-to-emitter, at Q1, causing the transistor to conduct heavily drawing sufficient current through the K1 MARK coil to overcome the no-input bias. This action causes closing of the normally-open contact of K1. When this happens, -12 vdc (pin 4) is routed (via the relay arm) through the normally-open contact, and out to PC board pin B as 1 logic.

Resistor R3 limits base-to-emitter current through Q1 to a safe value; diodes CR1 and CR3 prevent component damage by back EMF from the K1 field collapse. Network R1, C1 forms a spark suppressor, and CR2 provides TTY line isolation, while establishing the same common reference for both TTY line and keyer circuitry.

e. UNIT 2; 2A9 TIMING CIRCUIT (See figure 5-21). - Timing circuit 2A9 produces the timing pulses by which the entire unit is paced, and converts incoming serial TTY codes to parallel bits. The 2A9 receives +12 vdc (pin 20), -12 vdc (pin 4), ground (pins 1, A, Z, 22), serial TTY code input (pin 2), shift-inhibit input (pin 21), and clock reset input (pin N) and produces the following: clock monitor output (pin R), five parallel bit outputs (pins 10, M, 15, 16, P), driver/gating reset output (pin H), shift reset outputs (pins 18, 19), shift-inhibit enable (pin Y), and clock-reset enable (pin 12). The 2A9 Timing Circuit consists of: input buffer Z3; clock-control flip-flop Z2; timing generator (clock) Z1; single-shot multivibrator Z4; two discrete - component diode gates R3, CR1, CR2 and R4, CR3, CR4; shift register Z5 through Z9; and shift-reset output buffer Z10. Incoming serial TTY code input from 2A2 develops MARK (-12 vdc) and SPACE (0 vdc) voltages across R5 and passes through Z3, where internal logic levels of 0 vdc (0 logic, SPACE) and -10 vdc (1 logic, MARK) are established. Output of Z3 (TP4) is applied to both the Z2 SET input and the CR2 anode. Clock-control flip-flop Z2 is set by the positive-going excursion of the TTY input start pulse (all flip-flops in this unit trigger only on positive-going levels), and delivers a 1 to the Z1 enable input (TP7) starting the clock. This action produces timing pulses, at TP6 and TP1, of a width and repetition rate determined by R1, C1, and C2 (plus C4 and C5, if 45.45 baud operation is desired instead of the 74. 2 baud rate).

Clock output at TP6 toggles Z5, which, together with Z6, Z7, Z8, and Z9, forms a shift register sequentially enabling bit gates 1 through 5 in Z8 and Z9. In addition, the driver/gating reset gate is enabled during the fifth bit, so that a positive-going level will result at the end of the fifth bit, for use by various driver and gating circuits external to 2A9. For a detailed explanation of shift register operation, refer to paragraph 4-3p. Relevant test points within the shift register are TP6 (clock output), TP8 (Z5, 0 output), TP9 (Z5, 1 output), TP10 (Z6, 0 output), TP11 (Z6, 1 output), TP2 (Z7, 0 output), and PC board pins H, 10, M, P, 15 and 16 (gate outputs). While the bit gates are being sequentially enabled by clock output at TP6, serial code bit information is applied to these gates in the following manner. The TP1 output of Z1 lags the TP6 output of Z1 by a half-pulse length; therefore, a positive-going edge occurs at TP1 exactly in the middle of each pulse at TP6. This delayed output is applied to single-shot multivibrator Z4, where the positive-going edge causes it to produce a negative-going spike (1 logic) of 6 microseconds duration (determined by C3) in the exact middle of each TP1 pulse. These spikes are observable at TP3, and are applied to CR1 anode, enabling the CR1, CR2 gate for the duration of each spike. The other input to this gate is serial TTY code bits (TP4). Gate output, therefore, consists of a six-microsecond sample of the center of each MARK pulse input (TP5), and is applied to the bit gates for conversion to parallel.

The clock-stop sequence begins at the end of the 6th timing pulse; Z7 clears, placing a positive-going edge at PC board pin Y setting flip-flop Z2 of 2A8. Simultaneously, the 0 output of 2A8Z2 is routed back into 2A9 (pin 21) and is applied to the anode of CR4, toggling Z6 to 0. Z6, in turn, clears Z7, and both Z6 and Z7 are held in a reset condition by 2A8Z2 acting through the CR3, CR4 gate. Meanwhile, Z5 continues to toggle with each pulse from Z1, applying its 1 output to the CLEAR input of 2A8Z2 (2A9 pin 2). The next positive-going edge from the Z5 1 output occurs at the end of the 8th timing pulse, clearing 2A8Z2. Upon clearing, 2A8Z2 delivers a positive-going edge to clock-control flip-flop Z2 on 2A9 (pin N). Z2 clears, removing the enable from Z1, thus stopping the clock until the next TTY code input is received.

Shift-reset buffer Z10 consists of two buffers with paralleled inputs. These buffers carry the 1 output of Z7, and apply their outputs to PC board pins 18 and 1 for use by Shift Registers 2A6 and 2A7, to reset themselves at the end of each character. Test Data for Timing Circuit 2A9 is found on the Unit 2 timing chart (figure 4-3).

f. UNIT 2; 2A8 TIMING CIRCUIT (See figure 5-19). - Timing circuit 2A8 performs the following functions: (1) "E" character recognition; (2) Sequential parallel-to-simultaneous parallel code conversion; (3) fan-out of bit and reset information; and (4) clock reset. The 2A8 receives +12 vdc (pin 20), -12 vdc (pin 4), ground (pins 1, A, Z, 22), bits 1 through 5 sequentially (pins F, L, T, W, X), reset pulse (pin 11), and various clock-control inputs (pins 21, 17; refer to paragraph 4-3e) and produces the following: bits 1 through 5 simultaneously, fanned-out 2-for-1 (bit 1, pins 7 and J; bit 2, pins C and E; bit 3, pins D and B; bit 4, pins M and S; bit 5, pins R and N); buffered reset pulse, fanned-out 2-for-1 (pins 5 and 10); triggered 15 microseconds reset pulse, fanned out 8-for-1 (pins 12, 13, 14, 15, 16, 18, 19 and P); "E" character gate output (pin 2); and clock-reset outputs (pins Y and 3; refer to paragraph 4-3e). The 2A8 Timing Circuit contains: 5 quadruple buffers Z9, Z11, Z12, Z13, and Z14; one buffer Z8, 6 flip-flops Z2, Z3, Z4, Z5, Z6, and Z10; one single-shot multivibrator Z7; and one 9-input AND gate Z1 of which 6 inputs are used.

Bit information enters 2A8 in parallel, but sequentially; i. e. although each bit enters on a separate line, if bit 1 is present it would arrive before bit 2, which in turn would arrive before bit 3, etc. 2A8 acts as a storage buffer, retaining each bit as it enters, so that all bits may be available simultaneously. This is accomplished by flip-flops Z3, Z4, Z5, Z6 and Z10 (bits 1, 2, 3, 4, 5, respectively). Consider bit code 10101 (TTY character "Y"); Z3, Z5 and Z10 are set by the incoming 1 bits, while Z2 and Z6 remain cleared. Thus, at the end of the fifth element, the entire code is available as a single unit; i. e. all elements appear simultaneously at the flip-flop 1 outputs (Z3, TP1; Z4, TP4; Z5, TP9; Z6, TP11; Z10, TP10). The 1 outputs are each routed to two paralleled-input buffers (contained in Z9, Z11, and part of Z12), creating a 2-for-1 fan-out. The buffer output appears at PC board pins as noted previously, for routing to various drive and gating circuits. The remaining flip-flop, Z2, on 2A8 is used to reset clock 2A9Z1. When Z2 resets the clock, it delivers this same reset pulse to the CLEAR input of Z3, Z4, Z5, Z6, and Z10, causing any of the flip-flops that had been set to simultaneously clear. For a detailed explanation of Z2 operation, refer to paragraph 4-3e.

In addition to code bit inputs, 2A8 also receives a reset pulse going positive at the end of the fifth bit. The positive-going input triggers single-shot multivibrator Z7, which produces a 15 microsecond-wide negative-going buffered pulse (TP3); (part of Z8, input; pin 3, output; pin 6). Buffered pulse output (TP2) is applied to the paralleled inputs of buffers Z13 and Z14, producing an 8-for-1 fan-out, which is routed out of the board for use by the projection display and frequency readout drivers.

The remaining function of 2A8 is "E" character recognition. The Z1 AND gate has six active inputs; one for each of the five code bits, and one for the reset pulse (1 output of Z2). When an E (binary 10000) is read back, Z3 will carry a 1 and the remaining code bit flip-flops carry 0; therefore, the 1 output of Z3, and the 0 outputs of Z4, Z5, Z6 and Z10 are connected to Z1 input. The 1 output of Z2 places an added condition on the gate; Z1 is satisfied if and only if there is an "E" code and Z2 is set. The gate is enabled (negative-going) at the end of the 6th element, when an "E" is present, and disabled (positive-going) at the end of the 8th element. Z1 output appears at PC board pin 2. Test data for 2A8 is contained on Unit 2 timing chart (figure 4-3).

g. UNIT 2; 2A6, 2A7 SHIFT REGISTER (See figure 5-17). - Shift registers 2A6 and 2A7 enable the readout displays in proper sequence so that a given piece of readback information is routed to the display designated for that information. 2A6 and 2A7 are enabled sequentially; first 2A7 operates, then 2A6. Since both circuits are identical, only 2A7 will be described in detail with some added notes relevant to 2A6. Shift Register 2A7 receives +12 vdc (pin 20); -12 vdc (pin 4); ground (pins 1, A, Z, 22); reset pulse (bits 3, 4, 5, and 6) from Z7 of 2A9 (pin T); "E" output (bits 7 and 8) from Z1 of 2A8 (pin R); and reset pulse (bit 5) from reset gate of 2A9 via 2A8 (pin 15); and produces the following: 8 sequential gating pulses (pins R, 6, B, 7, S, X, V, 21), 8 sequential reset pulses (pins E, D, 3, 2, 19, 18, 17, 16), and a register transfer pulse (pin P). The 2A7 contains 8 flip-flops (Z1 through Z8, inclusive), two quadruple buffers (Z10, Z11), and two quadruple AND gates (Z9, Z12).

The pulses received and produced by 2A7 carry no code information (code bits travel a different route to the display indicators), but indicate the presence of information to be displayed. The "E" character is the first character received of any readback sequence, signalling the start of the readback sequence. 2A8Z1 places a 1 at the Z1 SET input at the beginning of bit 7 of the E character. At the end of bit 8, this input goes to 0 (positive-going), setting Z1, and thereby placing a 1 at the input to one of the buffers in Z10 (TP2). Buffer output appears at PC board pin 7 and is routed to the driver for the first parameter to be displayed (in this case, 10 mc frequency readout), thereby enabling that driver and allowing code bit information relevant to the first parameter to be displayed in the proper form by the appropriate readout indicator. Buffer output is also applied as one input to an AND gate in Z9. The second (and satisfying) input to this gate occurs during bit 5 of the first character, placing a 1 at PC board pin E. At the end of bit 5, this input goes positive, causing a 1-to-0 transition, positive-going edge at pin E. This positive-going edge is used to clear the readout driver in preparation for the next readback sequence. However, although the driver has been cleared, the readout indicator will retain the current display until a new input arrives (during the next sequence). All information to be conveyed to the readout driver is contained in the first five bits; therefore, at the end of bit 6, a positive-going shift reset edge issued from 2A9 is routed through 2A8, and clears any flip-flops that are set on 2A7. In this case, Z1 is set; the positive-going edge clears Z1 and, in doing so, sets Z2, thus enabling the second readout driver in the readback sequence. Each successive reset edge causes a shift, enabling the proper readout driver, and disabling all others. As Z8 is reset, it delivers a positive-going edge to pin P, which sets the first flip-flop of 2A6. Shift register 2A6 then continues the shift in an identical manner to 2A7, for a total of sixteen readback functions. Pin P of 2A6 is not used; 2A6 receives all inputs of 2A7, except that the 2A7 register shift pulse is substituted for the "E" code. Test data for 2A6 and 2A7 may be found on Unit 2 timing chart (figure 4-3).

h. UNIT 2; 2A4, 2A5 FREQUENCY GATING CIRCUIT (See figure 5-15). - Frequency Gating Circuits 2A4 and 2A5 are identical, and each comprises three identical sections. Therefore, only one section of one board will be explained in full detail. 2A5 converts bits 2 through 5 to a 4-bit Binary-Coded Decimal, and stores these BCD digits until required by the readout indicators. The 2A5 receives +12 vdc (pin 20), -12 vdc (pin 4), ground (pins 1, A, Z, 22), code bits 2 through 5 (pins E, 19, J, Y) gating pulses (pins H, K, 21), and reset pulses (pins N, V) and produces the following: three sets of binary-coded decimal digits (BCD) in a 1, 2, 4, 8 sequence (bits 2, 3, 4, and 5 respectively), for application to the 10 mc, 1 mc, and 100 kc BCD-to-decimal decoder/display units (NIXIE tubes). Each section of 2A5 consists of 4 bit gates (4 binary bits are needed to reproduce decimals 0 through 9), and 4 flip-flops. Each gate output is connected to the SET input of its own flip-flop. All CLEAR inputs are tied together, and to a common input line.

The 1 bit does not appear on the 2A4 and 2A5 boards. Since the 0 through 0 decimals are reproducible with only 4 binary bits the 1 bit can be used to convey additional information. In this case, the 1 bit of the first two codes are used jointly by 2A3. It is thus necessary to clear both first and second parameter readout storage for each of the first two codes (pin N connections). Consider selection of decimal 3 in the 10 mc display; the 4-bit code presented 2A5 is 1100 (a 1 in the "one" place, and a1 in the "two" place, signifying existence of a 2 and a 1, or 3). Therefore, the 2 and 1 bits (pins 19 and E, respectively) of the 4-bit code, which are the 3 and 2 bits (respectively) of the original 5-bit TTY code, provide an input to their particular gates in Z1. The second input to these gates in Z1 is the gating pulse from 2A7, signifying that the proper point in the readback sequence has arrived for readout of the 10 mc parameter. During the fifth TTY bit input, the reset pulse from 2A9 places a 1 at the gates in Z1, satisfying (in this case) the two gates containing the 1 logic (TP1, TP3) until the end of the fifth TTY bit, at which time the gates are disabled. The resultant 1-to-0 transition sets Z4 and Z5, providing the necessary combination to illuminate the 3 digit of the display unit. At the end of the sixth bit, a positive-going reset edge from 2A7Z9 clears Z4 through Z7 inclusive, in preparation for the next readout input for that parameter. Test data for 2A5 appears on Unit 2 timing chart (figure 4-3).

i. UNIT 2; 2A3 MEMORY/LAMP DRIVER (See figure 5-13). - Memory/Lamp Driver 2A3 interprets the presence or absence of the 1 bit in the first eight TTY codes read back, as a receiver status indication, and energizes the various receiver status lamps accordingly. The 2A3 receives +12 vdc (pin 20), -12 vdc (pin 4), ground (pins 1, A, Z, 22), gating and reset pulses from 2A7 (gating pins 9, 10, 11, 13, 14, 15, K, S; reset pins D, J, L, M, T, U, V, 6), and bit 1 from 2A8 (pin 12) and produces various ground returns for status lamp voltage, depending upon receiver status (pins 6, 7, 9, 11 of Z9 and Z11). With the exception of the bit 1 for the first two characters received, 2A3 is substantially identical in operation to 2A4 and 2A5. Therefore, refer to paragraph 4-3h for a detailed explanation of circuit theory. The following discussion will encompass the minor differences between 2A3 and 2A5, and

will explain the operation of bit 1 for the first two characters.

The readout storage flip-flops in 2A5 and 2A6 drove the display units directly, the flip-flops in 2A3 drive inverters. Thus, for example, a 1-to-0 transistion (positive-going edge) at TP17 will set Z2, placing a 1 at TP14. This action causes a 0 (ground state) at PC board pin 21, thereby illuminating the AFC ALARM status lamp. There is a minor exception to this in the driver comprising Z5 and Z14. This circuit, when activated, lights the DECODER POWER lamp, signifying loss of readback and/or a power-off condition of the remote receiver's memory unit. Since Z14 is a NOR gate, either a SET at Z5 or a sustained 1 at PC board pin 18 will cause a DECODER POWER indication (pin 18 receives clock-control flip-flop 2A9Z2 reset output. Therefore, a 1 on the 2A9Z2 reset side means that the clock is stopped. R1, C1 form an RC timing circuit, requiring the clock to remain stopped for a longer-than-normal interval, before enabling Z14.

Memory/Lamp Driver 2A3 uses the 1 bit of the first two readback characters to produce a tuning/ready/fault indication. Z7, in conjunction with Z3 and Z4, forms a binary comparator in which bit 1 of character 1 is compared with bit 1 of character 2. The resultant output ground causes the proper lamp to illuminate; indicating TUNING, READY, or FAULT status. For example, a 1 at TP12 and a 0 at TP4 sets Z4 but not Z3. The Z4 1 output (TP10) appears as one input to two AND gates in Z7. The Z3 reset side places a 1 at the remaining input to one of the two Z7 gates (TP2), satisfying the gate, and placing a 1 at the input to an inverter in Z11 (TP1). This causes a ground at PC board pin 3, providing a return for -12 vdc through the TUNING lamp. By the same process, a 0 at TP12 and a 1 at TP4 will light the READY indicator, and a 1 at both TP12 and TP4 will cause the FAULT lamp to illuminate; the combination of two 0's is not used for this particular function. Test data for 2A3 comprises its associated timing chart, and the timing charts for 2A7 and 2A8.

j. UNIT 2; 2A14, 2A15 MEMORY/GATING CIRCUIT (DUAL 4-POSITION) (See figure 5-25). - Memory/Gating circuits 2A14 and 2A15 utilize bits 2 through 5 to provide various ground returns for the AGC speed projection readouts. Each board contains two identical sections, and both boards are identical. Furthermore, each section within a board is nearly identical in operation to the bit 1 binary comparator in 2A3. For a more detailed explanation of the 1-bit comparator, refer to paragraph 4-3i.

The only difference between the comparator in 2A3 and the comparators in 2A14 and 2A15 is that the 2A3 comparator utilizes the same bit of two successive characters, whereas the 2A14 and 2A15 comparator sections utilize two successive bits of the same character. Within 2A14 or 2A15, the uppermost comparator (as shown in figure 5-25) uses bits 2 and 3 and the lower section uses bits 4 and 5 of the input code. Bit 1 is used by the comparator in 2A3. Capacitors C1 through C4 suppress switching transients. Test data for 2A14 and 2A15 comprises the timing chart for Unit 2 (figure 4-3).

k. UNIT 2; 2A1, 2A16 MEMORY/GATING CIRCUIT (SINGLE FUNCTION, 12 POSITION) (See figure 5-9). - Memory/Gating Circuits 2A1 and 2A16 utilize bits 2 through 5 to provide various ground returns for MODE projection and for equipment selection indicators. Although up to twelve separate indications per board are possible, the MODE circuit (2A16) makes use of only five indications and the equipment selection PC board (2A1) uses ten positions. Both 2A1 and 2A16 are essentially extensions of 2A14 and 2A15; however, 2A14 and 2A15 use two successive bits per section to display up to four possible "settings" for a given function, 2A1 and 2A16 utilize all four bits (bits 2 through 5 due to their greater capacity (up to twelve possible settings per function). Because the principles of operation of 2A1 and 2A16 are identical to that embodied in 2A3, refer to the discussions for both the 2A3, and 2A14 and 2A15; paragraphs 4-3i and 4-3j, respectively.

Memory/Gating Circuits 2A1 and 2A16 receive +12 vdc (pin 20), -12 vdc (pin 4), ground (pins 1, A, Z, 22), bits 2, 3, 4, 5 (pins J, M, L, 12), gating pulse from 2A7 (pin K), reset pulse from 2A7 (pin 3), shift reset from 2A9 via 2A8 (pin H) and produces keyed grounds to the proper projection readout indicator or to Unit 1 (pins N, 10, P, C, 13, 17, 15, 14, U, 21, Y, 19; not all of these need be used. Test data for 2A1 and 2A16 appears on Unit 2 timing chart (figure 4-3).

l. UNIT 3 (C-7775/UR); 3A1 POWER SUPPLY BOARD (See figure 5-32). - Power supply board 3A1 contains two sections, one providing + 12 volts regulated and the other -12 volts regulated. Input to each section is 18 vac from one of the secondary windings of power transformer 3T1. Because both sections are similar in operation, only the +12 vdc section need be fully explained; the differences between the +12 vdc and -12 vdc will also be noted. Unless preceded by the unit number, all reference designations refer to components physically mounted on A1; thus, C7 in the following explanation refers to 3A1C7; 3C7 would refer to a component mounted external to 3A1.

Incoming ac (pins B and 2) is rectified by full-wave bridge rectifier CR1, and passes through a surge limiter consisting of R7 and R8. The resultant pulsating dc is applied to pin 3 of Z1 which is an integrated voltage regulator, incorporating current limiting and short-circuit overload protection. Essentially, Z1 functions as an operational amplifier with heavy feedback. An output of Z1 is applied to the base of driver Q2. Driver Q2, along with R1, forms a divider-bias network for series-pass transistor Q1, which performs the actual regulation. The collector-emitter path of Q1 is in series with the filtered output of CR1 (filtering is accomplished external to 3A1 by capacitor 3C1, connected between board pin D and ground); Q1 thus acts as a series resistance, varied by Z1, via Q2. Therefore, voltage output is ultimately regulated by Z1. To regulate properly, however, Z1 must have an error input; this input is obtained by

sampling the output voltage at the junction of the voltage divider formed by R4 and R5. The error sample is applied as feedback input to terminal 6 of Z1. Within Z1, the error input is compared with an internal voltage reference standard in what amounts to a differential amplifier; output of this amplifier is applied to the base of Q2. Capacitor C4, connected between terminals 6 and 7 of Z1 is part of an internal frequency compensation network, to prevent oscillation at high frequencies and/or transient "ringing". Capacitor C1 bypasses stray pickup, and resistor R9 is an output bleeder. Resistor R10 and capacitor C3 are part of the dc reset line.

Current limiting is accomplished by Z1 in conjunction with resistors R6, R2, and R3. Limiting is of the "switchback" type, i.e. when a heavy current overload occurs, the switchback limiter reduces current flow to a relatively small fraction of maximum output, instead of simply limiting current flow to the maximum design value until the overload is removed. Limiter operation is as follows: Output current creates a voltage drop across R6, which would appear between Z1 terminals 1 and 8; however, the divider composed of R2 and R3 causes another voltage drop; this drop bucks out the drop across R6. Consider the case of a short circuit at the output; R2 and R3 are effectively in parallel across the output, therefore, the voltage across the combination approaches zero and the bucking voltage is no longer generated. The heavy current through R6 causes a relatively large drop to appear between Z1 terminals 1 and 8; these terminals become the current-limiting input terminals. Voltage regulator Z1 immediately reacts by reducing forward bias on Q1 until output current returns to a safe predetermined value (in this case, about 0.5 amp). The combination of R2 and R3 also provides a pre-load on the output of about 20 ma, so the regulator will always operate into a load. Terminal 4 of Z1 is ground input for the IC; terminal 5 of Z1 is connected to ground through by-pass capacitor C7. By-pass capacitor C7 reduces noise in the internal voltage reference source by the usual bypass action.

The -12 volt section of 3A1 functions in an identical manner to the +12 volt section, with the following exceptions: the -12 vdc series-pass transistor 3Q1 is mounted external to the board at pins 12 (emitter), 14 (collector), and21 (base); the surge limiter comprises resistors R19, R20, R21, and R22. Due to the polarity inversion, the current limiter bucking divider is connected between the surge limiter network and the junction of R14 and R15.

Resistors R10 and R11, and capacitor C3, form the dc reset circuit. The purpose of this circuit is to reset both Gating Circuit 3A4 and Shift Register 3A3 to a CLEAR (no code entry, clock stopped, shift register "zeroed") condition, upon initial application of power to the unit. Resistors R10 and R11 are in series between +12 vdc and -12 vdc board output, thereby forming a voltage divider; the potential across this divider network is 24 vdc. The resistances are in a ratio of 2.25 to 1.00, favoring the -12 vdc leg; therefore, the dc reset line, taken from the R10, R11 junction is held approximately 8 volts above -12 vdc, or -4 vdc with respect to ground. However R10 is shunted by C3 and upon initial power application, C3 presents a very low dc resistance until it charges, effectively short-circuiting R10 and immediately raising the dc reset line to +12 vdc. This positive-going pulse is used to reset the shift register and clock gating circuits, thus correcting any spurious triggering caused by initial power surges. As C3 charges, its dc resistance quickly rises to a nearly infinite value, effectively removing the short circuit from R10 and allowing the reset line voltage to fall back to -4 vdc. This action locks out the dc reset line until the equipment is shut down and then re-activated again. The dc reset is accomplished in approximately the first 100 milliseconds after power application.

m. UNIT 3; 3A6 KEYBOARD (See figure5-27). - Keyboard 3A6 is the man-machine interface by which the remote operator creates the proper program instructions for the generation and transmission of control commands to a properly-equipped receiver, at any distance. The 3A6 consists of 44 single-pole, make-and-break pushbuttons, all with one side connected to ground. The other side of each pushbutton is connected to an individual PC board pin of Code Register 3A5. Upon depression of a pushbutton, its associated 3A5 PC board pin is grounded. Except for two pushbuttons (3A6S13 and 3A6S14, labeled TUNE and CLEAR, respectively), each button is of the lock-out-detent type; i.e. once a button is pushed past a detent point, it remains in the depressed position, mechanically locking out any other button. When another button is depressed, the first button will pop out to its normally-open position, preventing generation of more than one code at a time. As noted, there are two exceptions to this; the TUNE and CLEAR pushbuttons. When either of these is depressed, it will cause any other button to pop out but will not remain depressed; instead, as soon as finger pressure is released, it will itself pop out thereby clearing the keyboard. Certain pushbuttons share a common connection to a given pin of 3A5 (e.g. S11 and S40), since, to eliminate ambiguity, certain of the codes are re-used for different functions when preceded by the proper preparatory code. Keyboard 3A6 should be serviced and maintained in accordance with the procedures outlined in the applicable sections of the keyboards Maintenance Standards book.

n. UNIT 3; 3A5 CODE REGISTER (See figure 5-40). - Code Register 3A5 generates the TTY codes to be transmitted. The 3A5 receives -12 vdc from 3A1 via a diode gate in 3A4 and various grounds provided by the pushbuttons on keyboard 3A6 and produces the proper combination of 1 and 0 outputs on the code bit lines to 3A4. Initially, -12 vdc (1 logic) is applied to each of the five bit lines (PC board pins 15, 3, Y, B, and F) of 3A5. Assuming no keyboard buttons are depressed, no grounds are provided to any of the 80 diodes in the matrix; in fact, one side of all diodes is left open, so that the static -12 vdc remains at each of the bit lines. Therefore, with no code to be generated, register output is 11111. Consider a ground at PC board pin 17, to provide the TTY code 10011; there is a unique combination of diodes for each possible character. For a 10011, bit 1 line is grounded through CR77, bits 2 and 3 lines are left open, and bits 4 and 5 lines are grounded through CR45 and CR61, respectively. However, this produces the binary invert of

10011 or 01100, at 3A5 output lines; this is done because another inversion will take place in shift register 3A3, thus restoring the original TTY code output.

The only components within Code Register 3A5 are 80 diodes, all MIL type 1N914. See the schematic diagram for an indication of the particular diodes and board pins involved in a specific character generation. Test data for 3A5 is found on Unit 3 timing chart (figure 4-2).

o. UNIT 3; 3A4 GATING CIRCUIT (See figure 5-38). - Gating circuit 3A4 starts and stops timing generator Z1 on 3A3, and delivers parallel code bits to the five TTY code gates on 3A3. The 3A4 receives +12 vdc and -12 vdc supply voltages from 3A1 (pins 20 and 4), dc reset from 3A1 (pin T), clock reset ("shift cycle complete") pulse from 3A3 (pin H), code bit input from Code Register 3A5 (pins C, 13, 9, 6 and 2), and ground (pins 1, A, 22, and Z); and produces timing generator enable/disable output (pin M) and parallel code bit output of 3A5 (tie-point), delivered to 3A3 (pins F, 10, 16, B and 8). Gating Circuit 3A4 consists of five-input discrete-component diode OR gate CR1 through CR5, buffer Z1, and flip-flop Z2.

Upon initial power application, 3A4 receives a dc reset pulse at pin T from 3A1, causing Z2 to unconditionally clear. If there is no TTY code being generated by 3A5; pins C, 13, 9, 6, and 2 of 3A4 each contain a 1, and output of the diode gate (TP2) is a 1. This output is applied directly to the input of buffer Z1 (pin 3 of Z1), which prevents false triggering of Z2 due to current sinking effects. Output of Z1 (pin 11, TP1), under this "no-code" condition, is a 1 which is applied to the SET input of Z2; Z2, however, triggers only on a positive-going edge (1-to-0 transition) and therefore will not set. Once a button on keyboard 3A6 is depressed, one or more of the TTY code bit input lines goes to zero, causing gate output (and thus buffer output) to also go to zero. This 1-to-zero transition constitutes a valid trigger pulse for Z2, and it sets placing a 1 at PC board pin M to enable the timing generator in 3A3. When 3A3 has completed its shift cycle, a reset pulse (1-to-0 transition) is delivered to 3A4 pin H; pin H is connected to the CLEAR input of Z2. Z2 clears, removing the timing generator enable from pin M, and will not set again until a change in TTY code input occurs.

The only discrete components on 3A4 are diodes CR1 through CR5 (comprising the diode gate), and gate load resistor R1. Test data for Gating Circuit 3A4 are contained on Unit 3 timing chart (figure 4-2).

p. UNIT 3; 3A3 SHIFT REGISTER (See figure 5-36). - Shift Register 3A3 converts parallel code bits from Code Register 3A5 into a serial pulse TTY code that is fed to Keyer 3A2, then via CCL link to the remotely controlled receiver. The 3A3 receives the following inputs: +12 vdc (pin 20), -12 vdc (pin 4), ground (pins Z22, A, and 1), dc reset (pin U), code bits 1 through 5 (pins B, H, 8, 12, 13, respectively), and timing generator enable (pin C). Outputs of 3A3 are serial TTY pulse train (pin V), and timing generator reset/disable. Shift Register 3A3 contains output gate Z9, which combines sequential code gate outputs into one common line output; code gates Z6, Z7, Z8 (dual units); start pulse plus five code bits, that carry the parallel bits to be sequentially enabled; flip-flops Z2, Z3, Z4, and Z5, which do the actual sequencing of the gates; timing generator Z1 (clock), that causes the sequencing to occur at a constant, predetermined rate; and discrete component diode gate CR1, CR2, R2.

Negative logic levels are used; i.e. "0" state = 0 volts, "1" state = -12 volts, switching occurs on a positive-going input. Initially, flip-flops Z2, Z3, Z4 and Z5 are all cleared ("0" state) by the dc reset pulse from 3A1, applied to the reset terminals (pin 1); these flip-flops (with the exception of Z5) have their SET (pin 8) and CLEAR (pin 3) terminals tied together, causing the flip-flop to "toggle," (i.e. change state every time a trigger pulse is applied to the tied-together terminals, referred to as the toggle input). Code gates Z6, Z7, Z8 (dual four-input AND gates) are initially inhibited. Code gate Z6 controls the start pulse and TTY code bit 1; code gate Z7 controls TTY code bits 2 and 3; and code gate Z8 controls TTY code bits 4 and 5. Output gate Z9, receiving no input, remains inhibited; and timing generator Z1, receiving no enable, is cut off. Depressing any button on keyboard 3A6 causes Code Register 3A5 to generate a five-bit parallel code. This code is applied (via gating circuit 3A4) to the five TTY code gates in 3A3; simultaneously, 3A4 places a 1 at pin C of 3A3, starting the timing generator. As long as pin C carries a 1, the timing generator (clock) will produce trigger pulses of 13.5 milliseconds duration at TP3 (for 45.45 baud operation, pulses are 22 milliseconds long; see timing chart, figure 4-2. When pin C goes negative (1 state), and as long as it remains in this state, TP3 will carry trigger pulse output of Z1. Consider depression of yellow FUNC button on 3A6; Code Register 3A5 generates and the code 10011 (CCIT character "B") is applied (via 3A4) to the five TTY gates. Simultaneously, 3A4 enables Z1.

The first pulse from Z1 (TP3) toggles Z2 to a SET condition; Z2 in turn, applies its 1 output (TP8) to an input of the start pulse gate (pin 3 of Z6), and places a 1 (-12V) at the anode of CR2 in the diode gate. A 1 at the CR2 anode causes a 1 to appear at the CR1 anode, thus placing a 1 at another of the four inputs of the start pulse gate (pin 1 of Z6). The third and fourth inputs to this gate are supplied by Z3 and Z4, respectively. Both these flip-flops are currently in a CLEAR condition (TP5, Z3; and PC board pin F, Z4), and supply output to the start pulse gate (Z6 pins 4 and 5) from their 0 sides. At this point, the start pulse gate is satisfied and delivers a 1 (TP1) to pin 1 of output gate Z9 (six-input NOR gate). Gate Z9 responds by dropping its output (pin 6) from its static level of 1 logic to 0 logic, thus providing a keyed ground (at PC board pin V) for use by Keyer 3A2. The second pulse from Z1 toggles Z2 back to CLEAR, disabling the start pulse gate (thus ending the start pulse), and placing a 0 at CR2 anode (TP8). A 0 at CR2 anode causes TP7 to go to 0 (a positive-going edge), thus delivering a valid trigger pulse to Z3. Flip-flop Z3 sets, placing a 1 at an input (TP6) to the bit 1 gate (pin 9 of Z6). As indicated, Z2 has cleared, and the output from its 0 side (TP2) becomes another of the four required inputs to the bit 1 gate (Z6 pin 7).

Flip-flop Z4, still CLEAR, provides the third of the four inputs; a 1 is delivered from Z4 pin 11 to Z6 pin 10, and is observable at PC board pin F. The remaining input to the bit 1 gate is the actual code bit from register 3A5 (via 3A4). In the code example under discussion (10011), the first bit is present and appears as 1 at Z6 pin 12. This satisfies the bit 1 gate, and it delivers a 1 (TP4) to pin 3 of Z9. The Z9 output (pin 6) drops from 1 to 0, appearing at PC board pin V for use by 3A2. The third pulse from Z1 again toggles Z2 to SET, thus removing a 1 from the bit 1 gate (and ending the bit 1 pulse) but does not clear Z3. This combination of a SET on both Z2 and Z3 places two 1s on two of the bit 2 gate inputs (TP8 and TP6 corresponding to Z7 pins 1 and 3). Flip-flop Z4 remains CLEAR and its 0 output places a 1 on the third input of bit 2 gate (Z7 pin 4, observable at PC board pin F). The final input to satisfy bit 2 gate would be the code bit; but in the 10011 example, this second bit is a 0 and the gate remains unsatisfied (logical 0 at TP9), thereby delivering a zero to pin 4 of Z9. The Z9 output at pin 6 remains 1, and appears at PC board pin V.

When Z2 set for the bit 2 gate readout, it again placed a 1 at the anode of CR2 (TP8), causing TP7 (toggle input to Z3) to become 1 (negative-going). Upon the Z1 fourth pulse, Z2 toggles to CLEAR, removing a bit 2 gate input (thus ending bit 2 readout) and returning CR2 anode to 0. This causes TP7 to return to 0 (positive-going) and toggles Z2 to CLEAR. When Z3 clears, its 1 output (TP6) goes to 0 (positive-going), triggering Z4 to SET. The combination of Z2 and Z3 being cleared, and Z4 being set, places a 1 at three of the four bit 3 gate inputs (TP2, TP5, TP13; Z7 pins 7, 9, 10); the fourth input is bit 3 itself. In the example used, the third bit is absent and the gate output is 0 (TP10) to pin 9 of Z9, causing the Z9 output to remain 1 (Z9 pin 6) and to appear at PC board pin V. The next (fifth) pulse from Z1 sets Z2, ending the bit 3 readout and places a 1 at CR2 anode (TP8). Flip-flop Z3 remains cleared, and flip-flop Z4 remains set. The 1 outputs from Z2 and Z4 (TP8 and TP13, respectively), and the 0 output from Z3 (TP5), place three 1s on three of the bit 4 gate inputs (Z8 pins 1, 3 and 4), with the remaining input being the code bit (Z8 pin 5). In the 10011 example, the fourth bit is present, satisfying the gate and producing a 1 at TP12. This 1 is delivered to Z9 pin 11 causing its output (Z9 pin 6) to go from 1 to 0, appearing at PC board pin V.

The sixth pulse of Z1 toggles Z2 to CLEAR, removing a 1 from the bit 4 gate (ending the fourth bit pulse) and placing a 1 on one input of the bit 5 gate (Z8 pin 7; TP2). When Z2 clears, CR2 anode (and thus TP7) goes to 0 (positive-going), toggling Z3 to SET and providing another input to the bit 5 gate (Z8 pin TP6). Flip-flop Z4 remains set, placing a third 1 on pin 10 of Z8 (TP13). The fourth input is the code bit (a 1 in the example), satisfying the gate, and placing a 1 at TP11 (Z9 pin 12). This again changes the Z9 output from static 1 state to 0, and appears at PC board pin V. The seventh pulse from Z1 again sets Z2, inhibiting the bit 5 gate (ending the fifth bit pulse) and placing a 1 at CR2 anode (TP8). Flip-flops Z3 and Z4 remain set (TP6, TP13), and Z5 remains cleared (as it has thus far). No gates are satisfied, and no output is therefore delivered to Z9 which retains a 1 at its output (PC board pin V). The Z1 eighth pulse clears Z2 causing a 0 at the CR2 anode (TP8); TP7 therefore goes to 0 (positive-going), toggling Z3 to CLEAR. When Z3 clears a 0 (positive-going) level at TP6 toggles Z4 to CLEAR; this produces a 0 (positive-going) level at TP13, toggling Z5 to a SET condition (PC board pin W). Again, no bit gates are enabled and Z9, receiving no input, holds a 1 at its output (Z9 pin 6, corresponding to PC board pin V). Flip-flop Z5, unlike Z2, Z3, and Z4, is not connected for toggle operation (its SET and CLEAR inputs are not tied together); therefore, although Z5 received a CLEAR input (positive-going level) every time Z2 cleared, Z5 was cleared to begin with and thus did not change its state. At this point, however, Z5 has been set, placing a 0 at CR1 anode.

When the ninth pulse issues from Z1, it toggles Z2 to SET, placing a 1 at CR2 anode (TP8); TP7 is held at 0 by the 0 from Z5 at CR1 anode. Flip-flops Z3 and Z4 remain cleared, and Z5 remains set. No code gates are satisfied, and the Z9 output remains at 1. The tenth pulse of Z1 clears Z2, producing a 0 (positive-going level) at TP8. Flip-flop Z3 will not toggle because TP7 has been held at 0 by Z5. The positive-going level at TP8 is delivered to the Z5 CLEAR input. Because Z5 was previously set, it now responds to a trigger pulse at its CLEAR terminal and clears. When Z5 clears, it places a 0 (positive-going level) at PC board pin W. This positive-going level is delivered to Gating Circuit 3A4, where it clears a flip-flop that in turn removes the enable from timing generator Z1, thus completing the character cycle. Note that all flip-flops and gates have been returned to initial conditions, awaiting generation of the next TTY character.

Capacitors C1 and C3, and C2 and C4 determine timing generator speed range (C1 and C2 only are used for 74.2 baud operation, C3 and C4 are added for 45.45 baud operation); potentiometer R1 sets exact timing generator rate within the range selected. L1 provides transient suppression to prevent false toggles, and resistor R2 is a load resistor for the diode gate. Test data for Shift Register 3A3 may be found on the Unit 3 timing chart, (figure 4-2).

q. UNIT 3; 3A2 KEYER (See figure 5-34). - Keyer 3A2 receives serial logic-level code bit inputs from Shift Register 3A3, and produces the contact closures necessary to key the external TTY line. The 3A2 receives -12 vdc (pin 4), +12 vdc (pin 20), keyed ground return from 3A3 (pin V), and constant ground (pins 1, A, 22, Z). Of these inputs, only -12 vdc and keyed ground return are used in this particular application. The Keyer, 3A2, is designed to provide dry contact closure to the line that will permit direct or inverted TTY keying. Current limiting resistors are incorporated, if required, between Y and X (Mark current condition) and U and X (Space current condition). K1, a mercury-wetted polar relay, has a "mark coil", and a "space coil". Depending upon which coil is energized, the relay connects COMMON pin X to either the MARK pin (Y and 21) or to the SPACE pins (R and U), through current-limiting resistors.

Keyer operation is as follows: -12 vdc enters 3A2 at pin 4 and is routed to one side of both coils of K1. The K1 mark coil is returned to ground through 470-ohm resistor R1, while the space coil receives a keyed ground return from Shift Register 3A3 (pin V). With either no code element or a MARK element (-12 vdc) present at pin V, no ground return is provided to the K1 space coil and it remains deenergized. The mark coil, however, is returned to ground through series resistor R1, and thus holds the relay in its MARK position. Therefore, if there is a prolonged absence of code inputs, K1 produces a MARK-HOLD condition on the TTY line to prevent associated equipment "running open". When a SPACE element occurs, pin V is raised from -12 vdc to ground potential, energizing the K1 space coil and thus closing the normally-open side of the relay. With no space input the relay returns to the MARK condition. Diodes CR1 and CR2, across each coil, bypass the Back EMF caused by magnetic field collapse and prevent damage to power supply and/or shift register components. Networks C1, R2 and C2, R3 suppress keying transients; resistors R4 and R5 are current-limiters for 20 ma operation, while R6 and R7 are current-limiters for 60 ma loops. PC board output pins R, U, X, Y, and 21 appear respectively at pins D, F, G, H, and E of rear-panel connector 3J2. Test data for 3A2 may be found on Unit 3 timing chart (figure 4-2).

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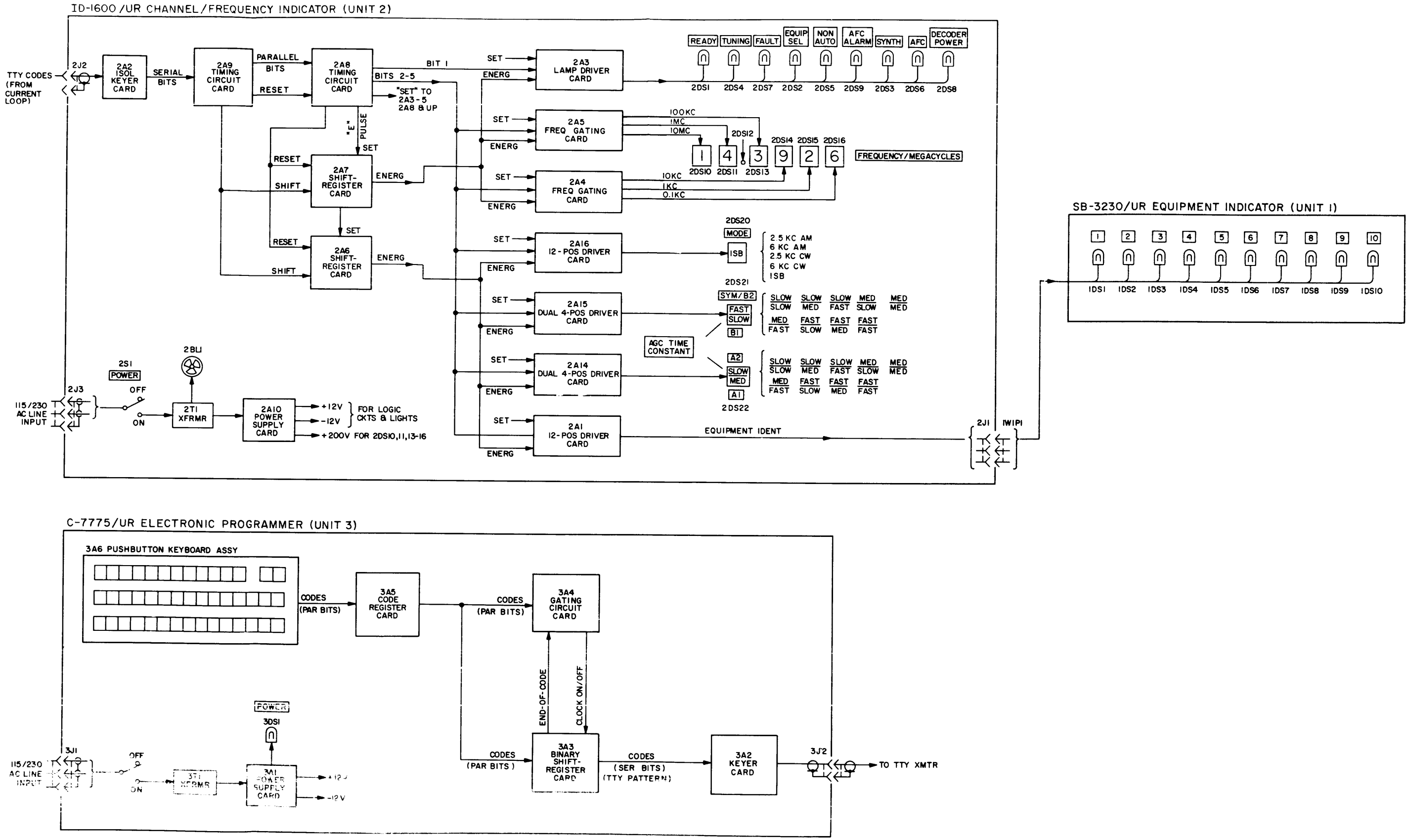

Figure 4-1. Overall Functional Block Diagram AN/URA-63

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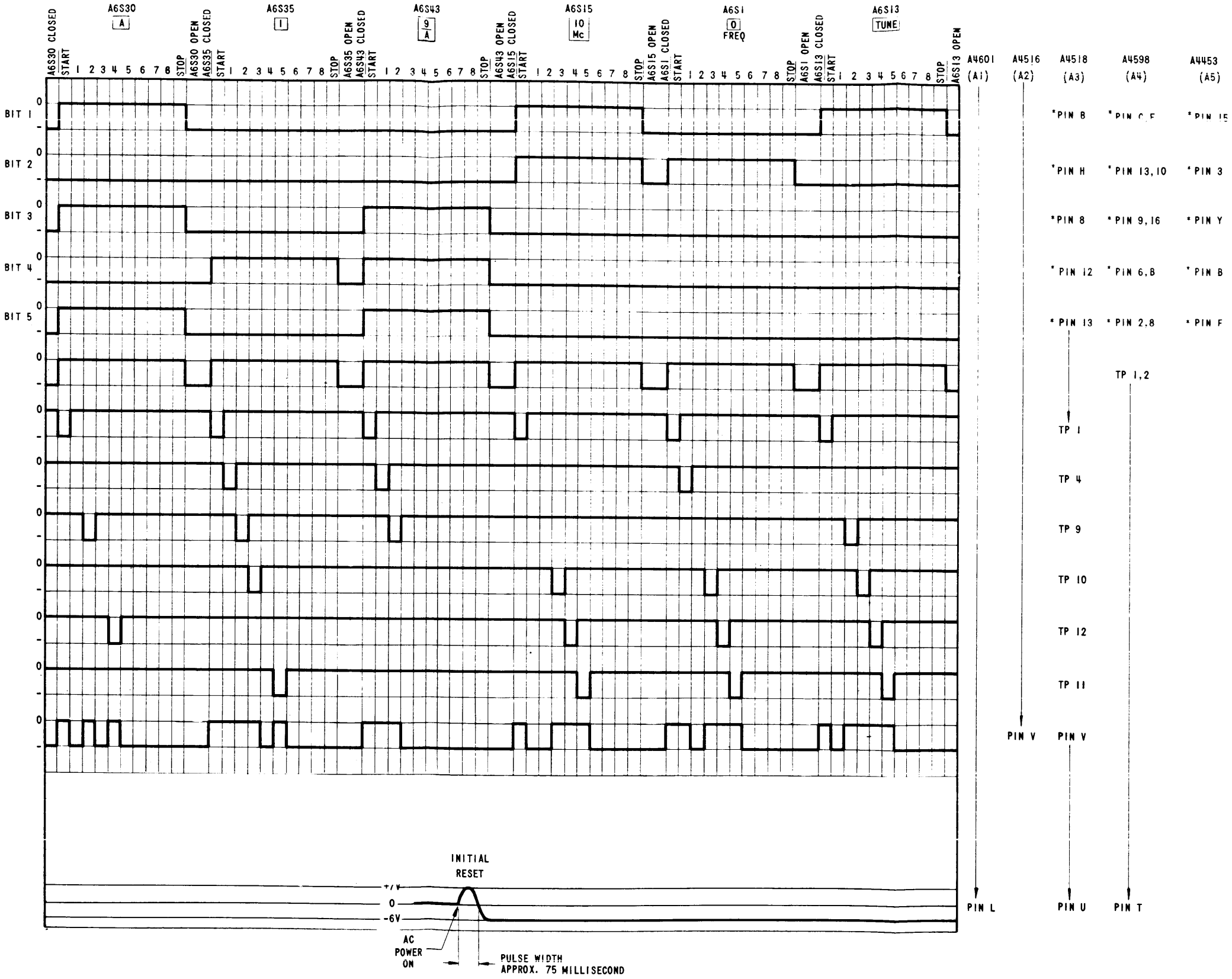

VOLTAGE & GROUND CHART

	-12V	+12V	GND	A.C.
A1	V,W,X,Y	F,H,J,K	1,A,Z,22	22VAC ACROSS B & 2 26VAC ACROSS N & U
A2 THRU A4	4	20	1,A,Z,22	

NOTES:

1. SINGLE INITIAL RESET PULSE OCCURS WHEN POWER SWITCH IS TURNED ON
2. NEGATIVE LEVELS ARE APPROXIMATELY 10 VOLTS
3. WAVE FORMS ARE SEEN ONLY WHEN TERMINATED WITH A 1.2K OHM RESISTOR TO NEGATIVE 12 VOLTS
4. TYPICAL TIMING SEQUENCE: SHOWN FOR 100 WPM

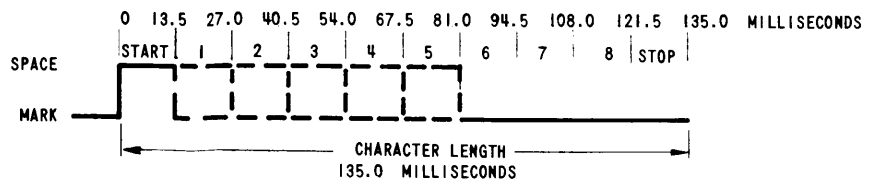

Figure 4-2. Timing Chart, Programming Section (Unit 3) AN/URA-63 (Sheet 1 of 2)

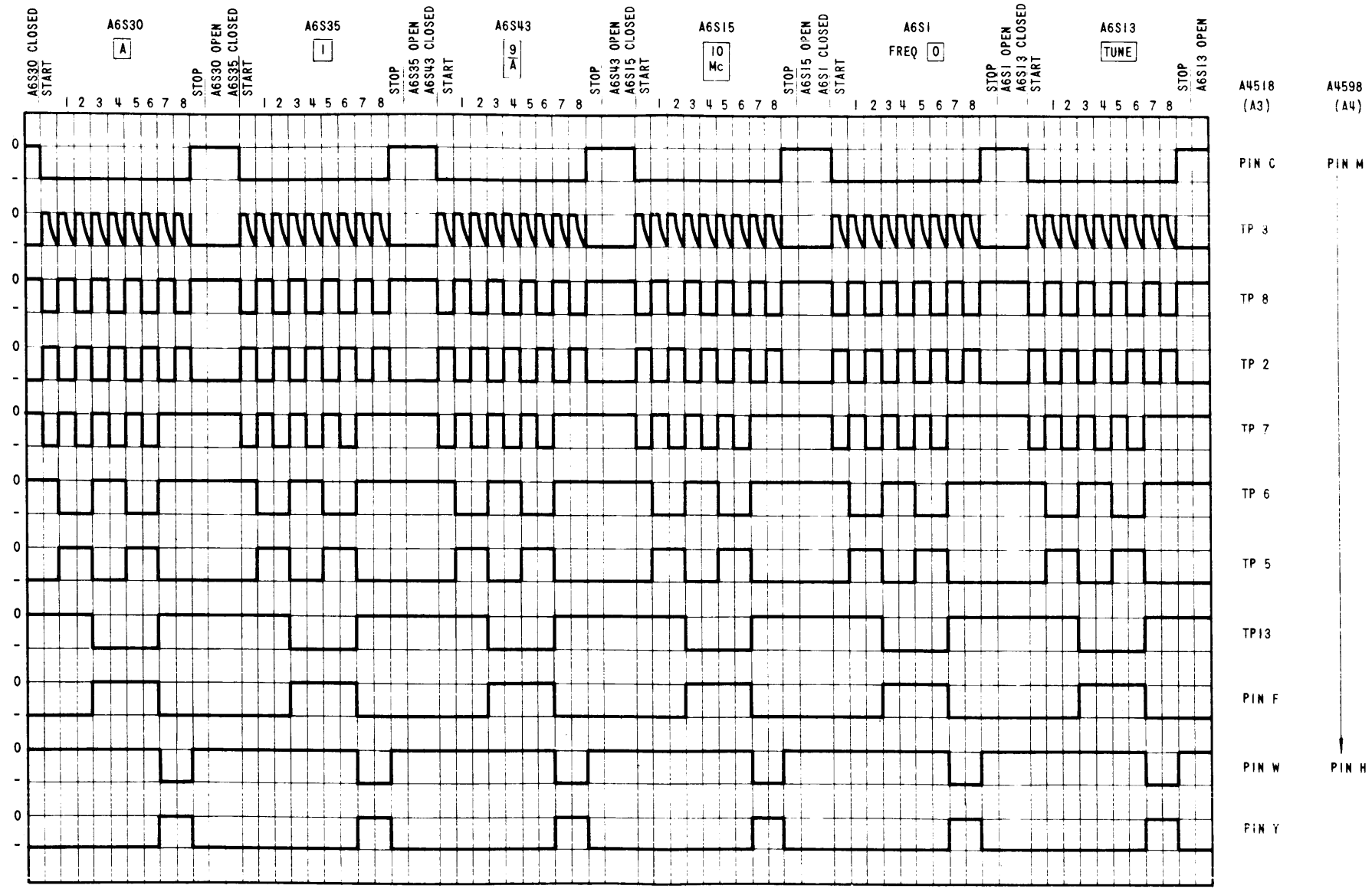

Figure 4-2. Timing Chart, Programming Section (Unit 3) AN/URA-63 (Sheet 2 of 2)

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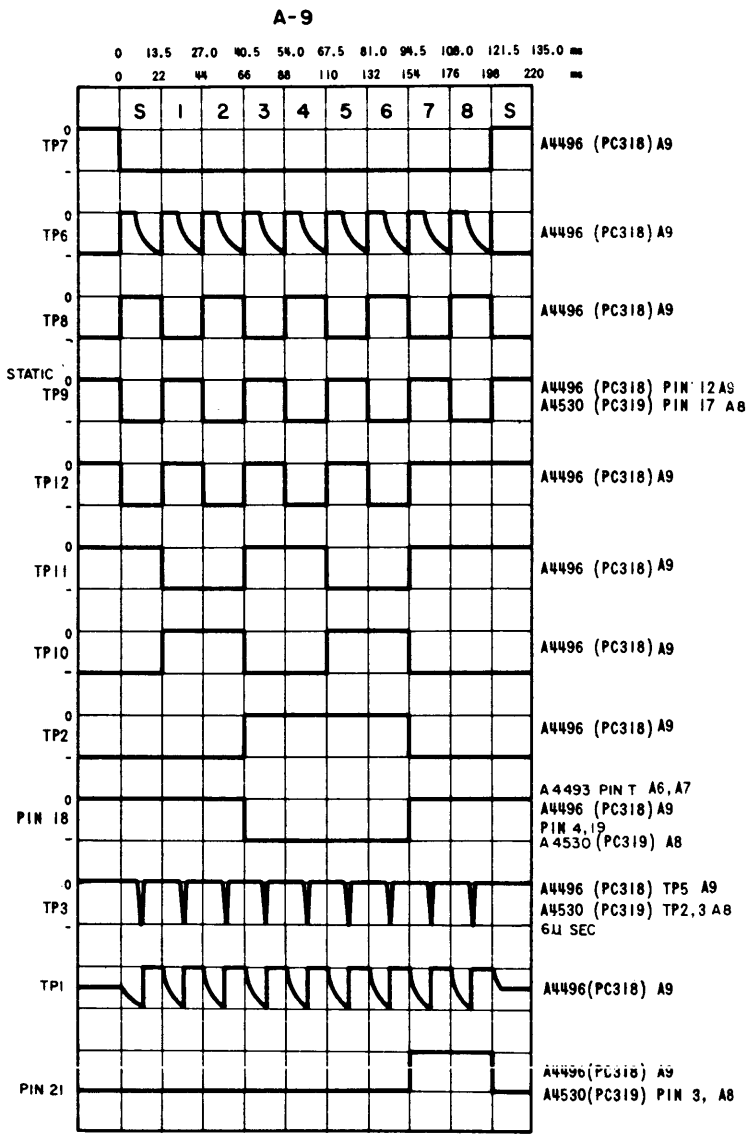

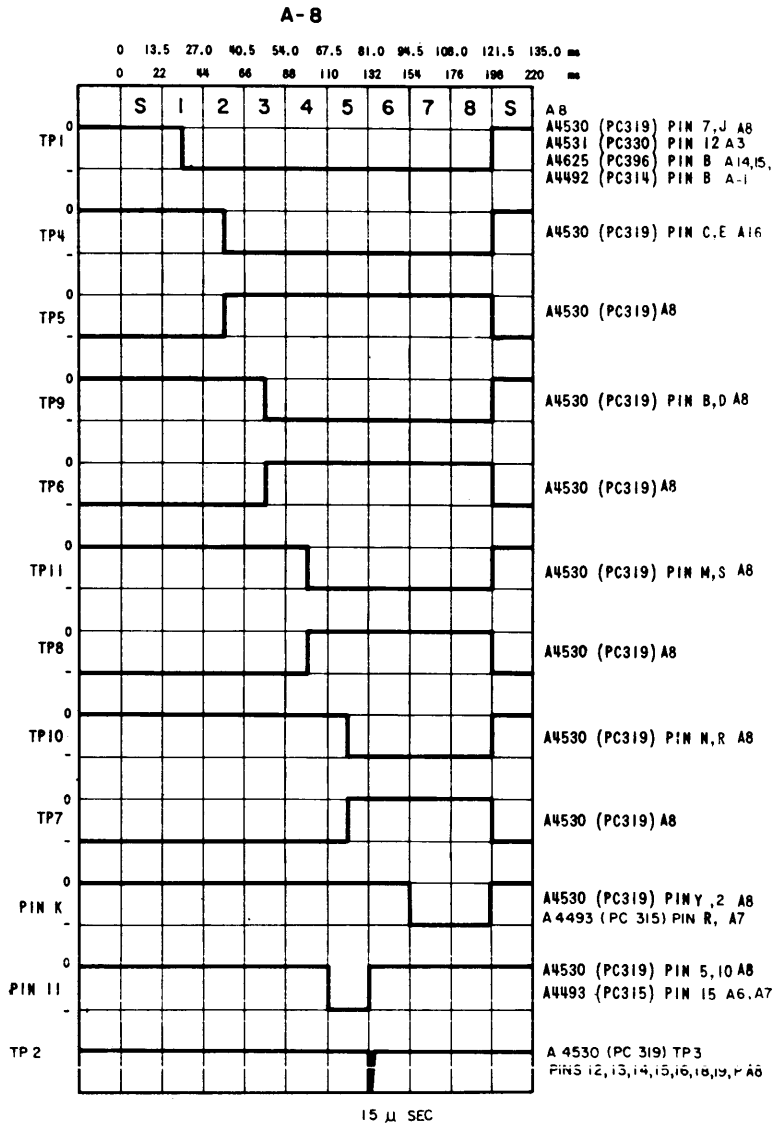

* NOTE: FOR WAVEFORMS DENOTED (*), THE NEGATIVE PULSES DRAWN IN SOLID LINES APPLY TO A-7 ONLY; THE NEGATIVE PULSES DRAWN IN BROKEN LINES APPLY TO A-6 ONLY.

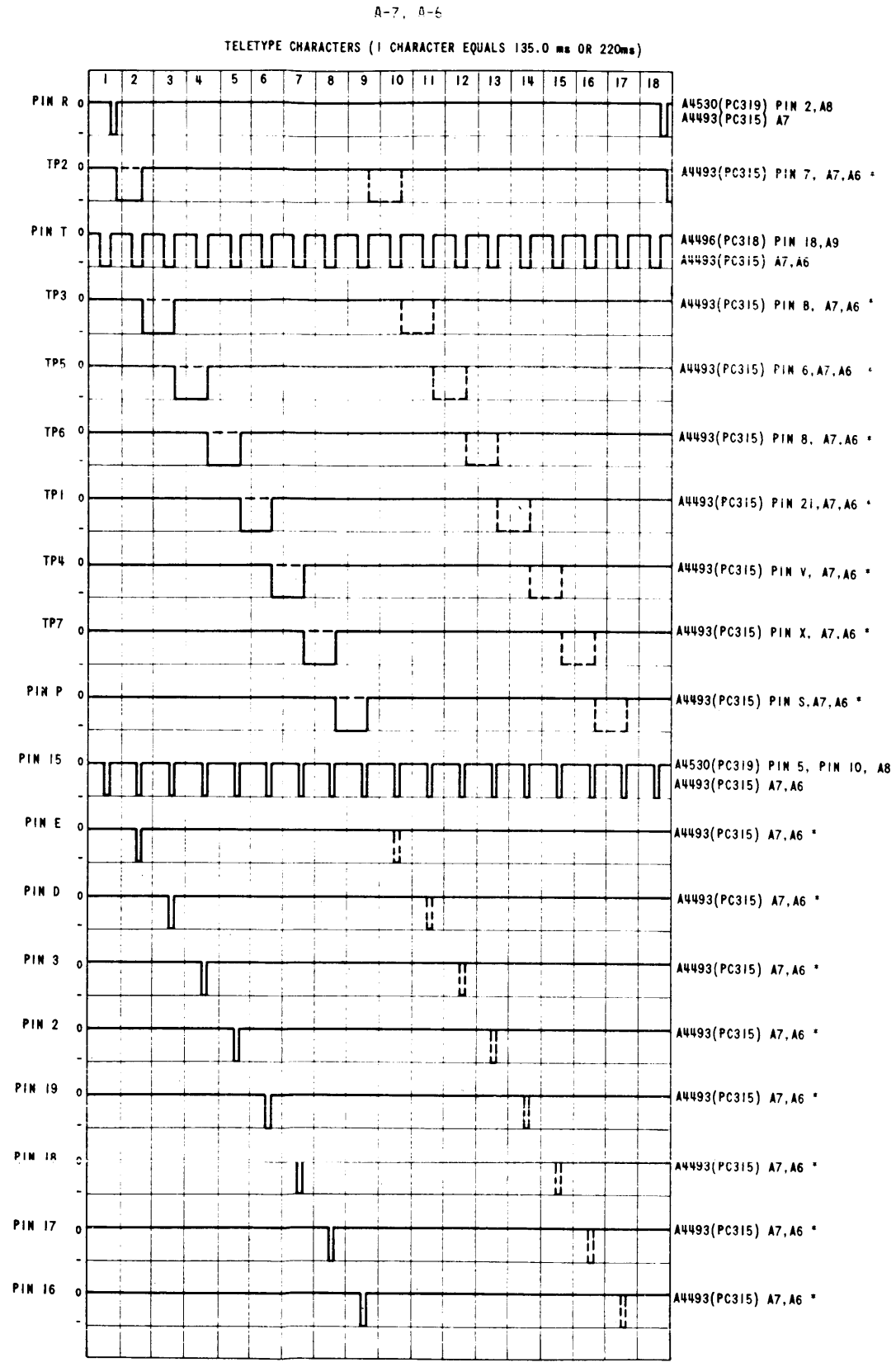

Figure 4-3. Timing Chart, Readback Section (Unit 2) AN/URA-63 (Sheet 1 of 3)

A-3

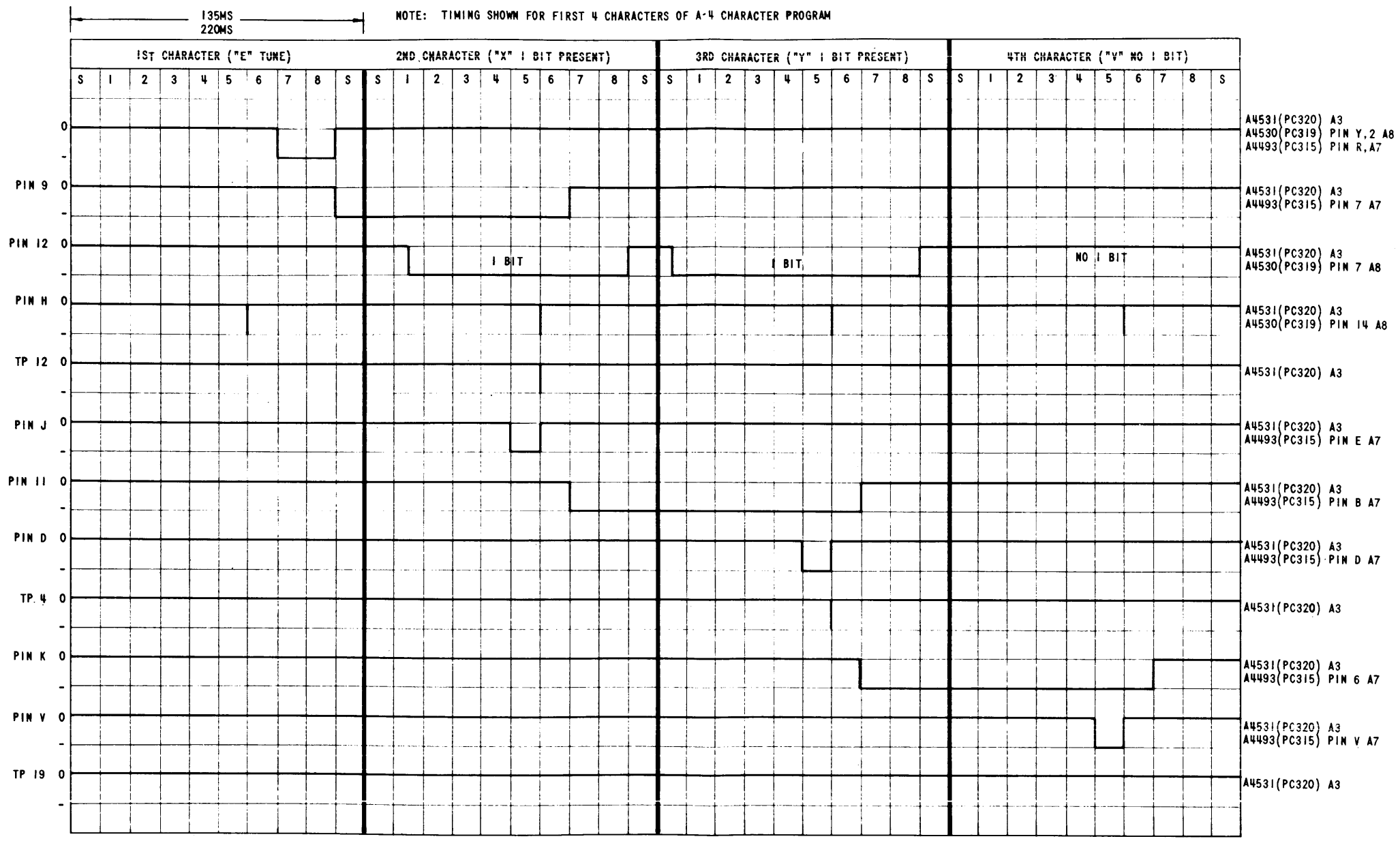

Figure 4-3. Timing Chart, Readback Section (Unit 2) AN/URA-63 (Sheet 2 of 3)

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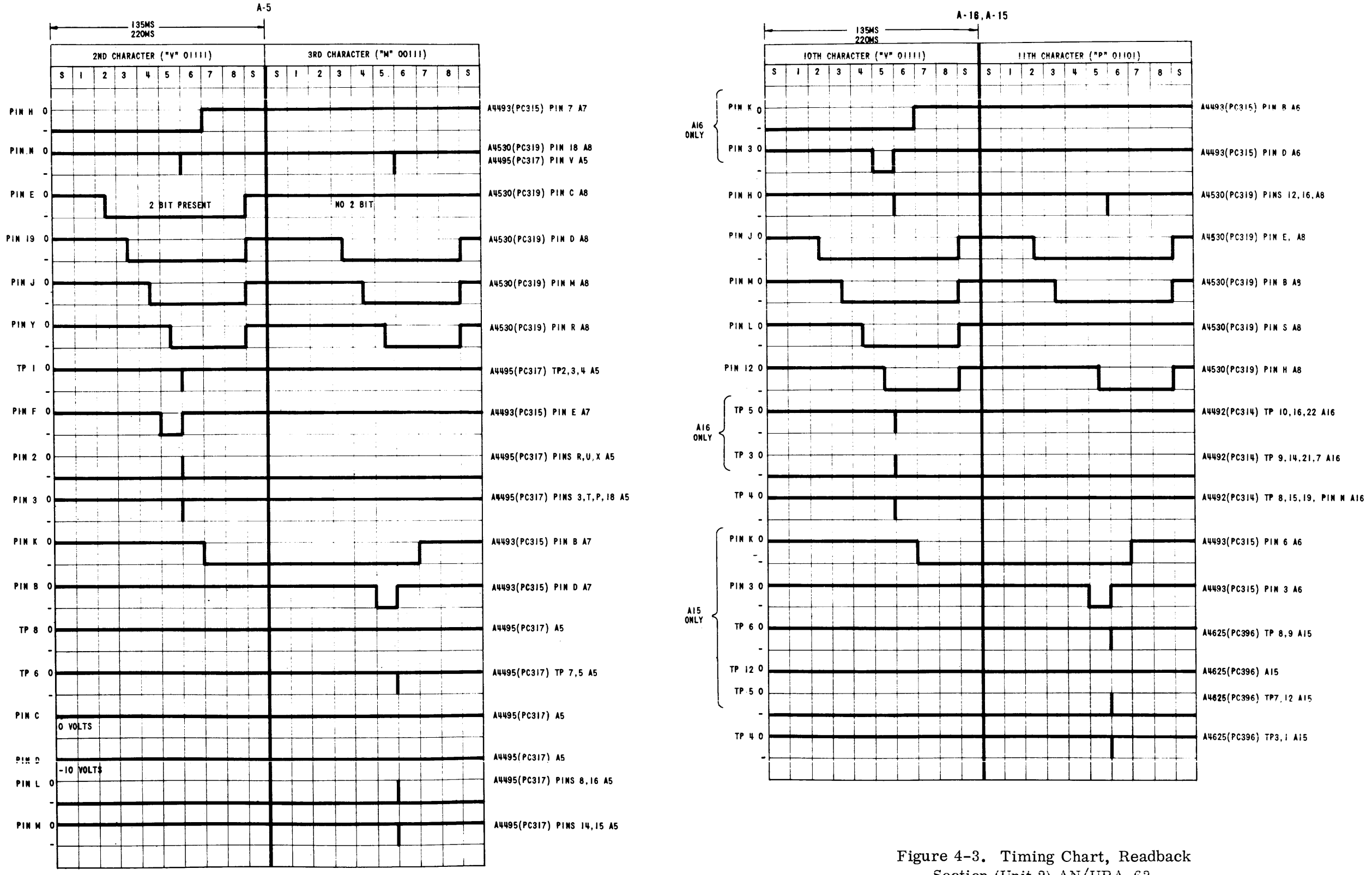


Figure 4-3. Timing Chart, Readback Section (Unit 2) AN/URA-63

(Sheet 3 of 3)

SECTION 5

MAINTENANCE

5-1. FAILURE, PERFORMANCE AND OPERATIONAL REPORTS.

Note

The Naval Electronics System Command no longer requires the submission of failure reports for all equipments. Failure Reports and Performance and Operational Reports are accomplished for designated equipments (refer to Electronics Installation and Maintenance Book, NAVSHIPS 900, 000) only to the extent required by existing directives. All failures shall be reported for those equipments requiring the use of Failure Reports.

5-2. PREVENTIVE MAINTENANCE.

For preventive maintenance procedure, test equipment and schedules, refer to the Maintenance Standards book for Remote Control Group AN/URA-63.

5-3. ALIGNMENT AND ADJUSTMENT.

a. TEST EQUIPMENT AND SPECIAL TOOLS. - Test equipment and tools that are required are listed in Table 1-5. Test equipment that is needed for each specific Test/Alignment will be listed as required.

b. SPECIAL JIGS. - There are no special Test Jigs used in the Testing/Alignment of this equipment.

c. ALIGNMENT AND ADJUSTMENT PROCEDURES, PROGRAMMER C-7775/UR (Unit 3).

(1) PRE-ALIGNMENT INSTRUCTIONS. - See figures 5-32, 5-33, 5-36, and 5-37 and perform the following procedures:

(a) Remove four screws holding the unit in the cabinet and pull the unit out of the cabinet until the slide locks click.

(b) Remove top cover to gain access to the Printed Circuit boards.

(c) Before making adjustment in the unit, check the Power Supply voltage.

(d) Adjust the timing generator. The timing in milliseconds will depend upon the Baud rate being used in the system; 74.2 Baud is standard, causing the pulses from the timing generator to be 13.5 milliseconds.

(2) TEST EQUIPMENT REQUIRED. - The test equipment needed for performance of the C-7775/UR procedures are Frequency Counter, AN/USM-207 and Miltimeter, AN/PSM-4C.

(3) CONTROL POSITION. - Set power switch to ON.

(4) ALIGNMENT PROCEDURE, 3A1 POWER SUPPLY.

(a) With the AN/PSM-4C, check the following voltages on the noted subassemblies test points (be careful to observe polarity on the meter); all voltage will be ±10%:

A1 -12 volts dc
+12 volts dc

(b) Set power switch to OFF position. With AN/USM-281A in dc function, connect scope probe to "DC RESET" test point. Set power switch to ON position observing oscilloscope screen. Observed dc reset level should rise to approximately +12 vdc and then fall and remain at approximately -8 vdc.

(c) Disconnect test equipment and set power switch to OFF position.

(5) ALIGNMENT PROCEDURE, 3A3 TIME GENERATOR (CLOCK) ADJUSTMENT.

(a) Connect a jumper from pin 4 (-12 vdc) to pin C (timing generator enable) of 3A3.

(b) Connect frequency counter to 3A3TP-2 and observe the clock period.

(c) Adjust 3A3R1 so that counter indicates 13.5 milliseconds ±0.2 milliseconds.

(d) Remove counter.

(e) Replace top cover on unit.

(f) Depress slide fastening buttons and push unit into the cabinet being careful that cable retraction is taking place correctly.

(g) Replace 4 screws to hold unit in cabinet.

d. ALIGNMENT AND ADJUSTMENT PROCEDURES, CHANNEL FREQUENCY/INDICATOR ID-1600/UR (UNIT 2).

(1) PRE-ALIGNMENT INSTRUCTIONS. - See the following schematic and assembly drawings and then perform procedures (a) through (d).

Figures 5-4 and 5-7 Unit 2
Figures 5-11 and 5-12 2A2 Isolation Keyer
Figures 5-21 and 5-22 2A9 Clock Timing Ckt.
Figures 5-23 and 5-24 2A10 Power Supply

(a) Remove four screws holding the unit in the cabinet, and pull out unit from cabinet until the slide locks click.

(b) Remove top cover to gain access to the Printed Circuit boards.

(c) When using the extender card, place card in the chassis sockets so that the test points on the extender card face toward the front panel of the unit. Only then will the test point identification coincide with the pin numbers and letters of the printed circuit boards.

(d) Adjust the timing generator. The timing in milliseconds for this unit will depend upon the Baud rate being used in the system. The 74.2 Baud is standard, causing the pulses from the timing generator to be 13.5 milliseconds. This standard will

be used in the alignment and adjustment procedure. The Teletypewriter used should be compatible to this standard and should be connected to the AN/URA-63 in a manner similar to that described in paragraph 3-4b; substitute AN/URA-63 for remote receiver.

(2) TEST EQUIPMENT REQUIRED. - The test equipment needed for performance of the ID-1600/UR procedures are: Oscilloscope, AN/USM-281A; Frequency Counter, AN/USM-207; Multimeter (VOM), AN/PSM-4C; Teletypewriter, TT-176/UG; and DC Loop Supply.

(3) CONTROL POSITIONS. - Set power switch in the ON position.

(4) ALIGNMENT PROCEDURE, 2A10 POWER SUPPLY (See figures 5-23 and 5-24).

(a) Using the AN/PSM-4C, check the following power supply voltages at the corresponding test points; marked on the 2A10 circuit board (be careful to observe polarity on the meter). Voltages should be ±10%.

+12V
-12V
+200V

(b) Disconnect test equipment and set power switch to OFF position.

(5) ALIGNMENT PROCEDURE, 2A2 ISOLATION KEYER (A4494) (See figures 5-11 and 5-12).

(a) Remove A2 from socket, place on extender card and return to socket.

(b) Set R4 fully counterclockwise.

(c) Externally trigger Oscilloscope, AN/USM-281A, with signal on pin 12 of 2A2.

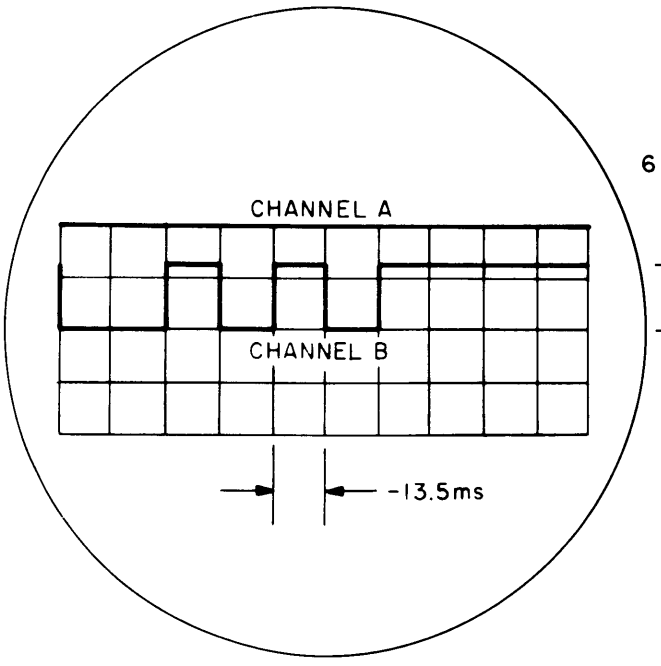
(d) Allow a free run trace on the scope by adjusting the stability and triggering level.

(e) Set up both channels on oscilloscope for dc inputs, and set volts/cm on Channels A and B for 5 volts/cm position with variable in calibrated position. Using vertical position controls, set zero reference for A and B sweeps. Set channel A sweep at the top of the screen for zero volts. Set channel B sweep at center of screen for zero volts.

(f) Connect ground lead of scope probe for channel B to pin 15 of 2A2 and the scope probe to pin 12 of 2A2. The channel B trace should go to +12 vdc. Reduce the stability on scope until trace just disappears.

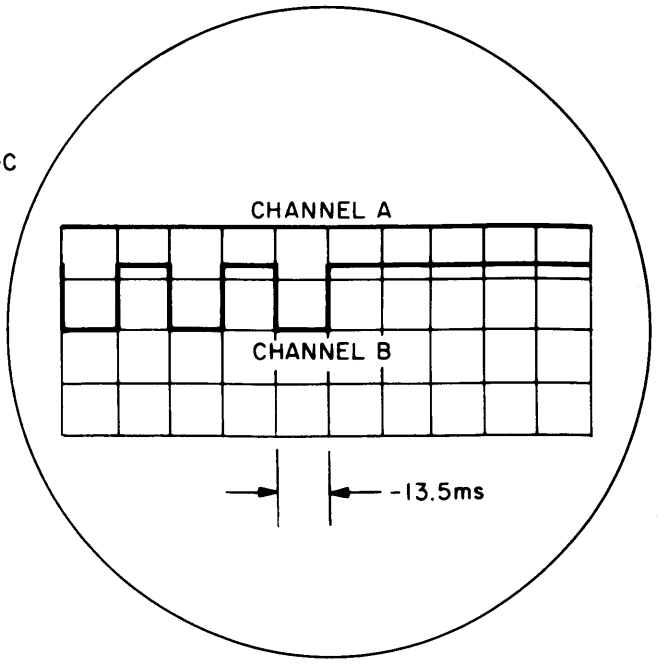
(g) Alternately send R's and Y's on the Teletypewriter keyboard to display their corresponding waveforms on the scope. (It may be necessary to adjust triggering level on scope to obtain waveform display.) Adjust the variable time/cm of the horizontal sweep on the scope until the pulse duration of a mark or space in the R and Y codes occupies 1 cm on the horizontal sweep of the scope for 13.5 millisec/cm or 135.0 millisec for the entire horizontal sweep. The following waveforms should be observed.

FOR A "R" CHARACTER



6 VDC

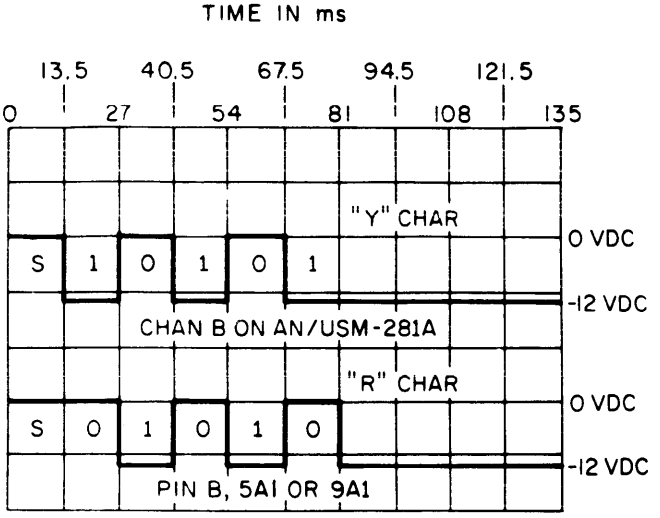
FOR A "Y" CHARACTER



(h) Turn power switch to ON position.

(i) Place scope probe for channel B on pin B of 2A2 (use extender card test point) and ground lead for scope probe to chassis ground. Set both scope channels volts/cm to 10; channel B sweep should be at -12 v.

(j) Continue to alternately send R's and Y's on the Teletypewriter keyboard and adjust R4 so that the pulse duration for a start, mark, or space pulse occupies 1 cm on the horizontal display of the scope.



(k) Remove scope probe and trigger input line from 2A2. Turn power switch to OFF position. Remove 2A2 and extender card from socket, and return 2A2 to its own socket.

(l) Disconnect Teletypewriter and DC Loop Supply.

(6) ALIGNMENT PROCEDURE, 2A9 CLOCK TIMING CIRCUIT (See figures 5-21, 5-22, 5-19 and 5-20).

(a) Remove 2A8 from chassis socket.

(b) Remove 2A9 from socket, place on extender card and return to socket.

(c) Connect jumper between pin 4 of 2A9 and TP4 on 2A9.

(d) Connect channel A scope probe to TP6 and ground lead to pin A of 2A9.

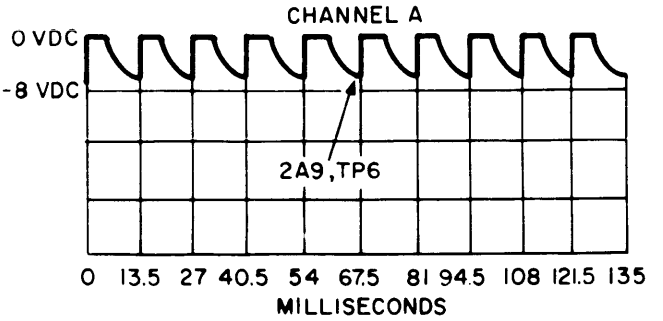
(e) Connect vertical signal output of Oscilloscope to AC Signal Input of Frequency Counter.

(f) On the counter set the function to 1 period average, time base to 10 microsec. and sensitivity volts RMS to . 1.

(g) Turn power switch to ON position.

(h) Allow a free run trace on scope by adjustment of stability. The pulse output of the Timing Generator Z1 will be displayed on the scope. The repetition time will be displayed on the counter.

(i) Adjust 2A9 R1 so that the pulse repetition time as displayed on the counter is 13. 5 millisec, and 1 pulse occupies 1 cm as displayed on the horizontal sweep of the Oscilloscope.



(j) Turn power to OFF position. Disconnect test equipment and remove jumper. Remove 2A9 and extender card from socket. Return 2A9 and 2A8 to their respective chassis sockets.

Note

After completion of alignment procedures; replace top cover on unit, and depress slide fastening buttons and push unit into cabinet being careful that cable retraction is taking place properly. Replace 4 screws to hold unit in cabinet.

5-4. REPAIR.

a. INTRODUCTION. - The following repair methods or procedures apply to assemblies or sub-assemblies whose removal, repair, and/or reassembly is not obvious. There are no special tools required for the repair of this system. A good low wattage desoldering kit should be used for the removal of Printed Circuit board components. A low melting point solder, such as 60/40%, will decrease the possibility of damage to new components due to too much heat being applied.

b. TEST EQUIPMENT AND SPECIAL TOOLS. - For the repair, removal, and replacement of units, sub-assemblies, and components; special test equipment and tools are not required. An adequate set of miniature solid state repair tools, though, should be a part of the standard tool box.

c. REPAIR OF CHASSIS COMPONENTS. - Power transistors are mounted on the chassis and heat sinks. When replacing these transistors use a standard type "Thermal Compound" between the transistor and its mounting where the compound was used before.

CAUTION

Be careful in removing transistors from the chassis and heat sinks. Between the transistor and its mounting there may be a mica or other type insulator. The mica/insulator must be used and in position when a new transistor is remounted.

d. REMOVAL, REPAIR AND REPLACEMENT OF PARTS, SUB-ASSEMBLIES AND WIRING.

(1) PRINTED CIRCUIT BOARDS.

(a) REMOVAL AND REPLACEMENT. - The various boards slide into the chassis on tracks and, when pushed down to the limit, engage female plugs and tension spring contacts. It is only necessary to grasp the board on both ends and apply pressure upward to disengage it. When plugging in a board take care to engage the phenolic card in the guide slots and exert even pressure downward to seat the card firmly. Some boards cannot be removed by finger pressure alone. A tool is supplied to assist in disengaging these cards.

(b) REPAIR. - Printed Circuit board repair requires special techniques in order to prevent damage to the board and its associated components. Reference should be made to NAVSHIPS 0967-000-0120.

CAUTION

There are transistors mounted on Printed Circuit boards which require heat sinks. If any of these transistors are replaced, reinstall heat sinks.

(2) WIRING. - If it is determined that a wire is defective and it cannot be repaired proceed as follows: Determine the origin of both ends of the wire. Disconnect or unsolder one end. With a AN/PSM-4C used as an ohmmeter, measure the resistance, from end to end. It should be 0 ohms. Unsolder or disconnect the other end and measure resistance again between both ends. If this wire is in a harness, remove it if possible. If the wire cannot be removed insulate both ends. Replace the wire along the same path as the original wire and use the same color and type.

CAUTION

Use the same size wire or a size larger, if necessary. Bind the wire to the harness as before.

(3) REMOVAL OF NON-REPAIRABLE 3A6 SWITCH ASSEMBLY (See figures 5-28, 5-31, and 5-43).

(a) Turn power to OFF.

(b) Remove four screws holding unit in the console.

(c) Pull unit out until it locks in the slides.

(d) Disconnect power from J1.

(e) Disconnect the dc loop from J2.

(f) Remove unit from Console and place it upside-down on a workbench.

(g) Remove bottom cover.

CAUTION

The removal of the below six screws will release and free entire switch assembly. Caution is to be used in its removal for maintenance and repair. Do not exert extreme pull or tension upon the cable harness and connected wiring.

(h) Remove six screws holding A6 switch assembly to the front panel, located beside A6S1, S14, S15, S29, S30, and S44 on the front panel (figure 5-28). (Plastic buttons do not have to be removed.)

(i) Carefully move switch assembly toward the rear of the unit in order to clear and remove pushbuttons from the front panel holes.

(j) Lift switch assembly upward to clear chassis.

CAUTION

Use a piece of cardboard or similar material between switch assembly and chassis to keep from damaging switch assembly and chassis components.

(k) Carefully identify and mark each wire connected to switch assembly before unsoldering.

(l) Unsolder all wires connected to assembly.

(m) Reassemble in the reverse order.

Note

Refer to emergency maintenance for repair or replacement of one of the individual switches and replacement of a row of switches.

5-5. EMERGENCY MAINTENANCE (See figure 5-43).

a. 3A6 SWITCH ASSEMBLY.

(1) Refer to removal of A6 switch assembly, paragraph 5-4d(3).

(2) After removing switch assembly from the front panel and before unsoldering and disconnecting any wiring, identify defective switch.

(3) Test individual switches before it is determined that replacement is necessary.

(4) If it is determined that a switch must be replaced, proceed as follows:

(a) There are three switches which are not normally used; A6-S27 through S29, figure 5-28. These may be used and/or removed for replacement. (See figure 5-43.) Remove screws 5 and 6.

(b) To replace a switch in row 3, the switch assembly A6 need not be removed. Remove the bottom cover and row 3 switches are accessible.

(c) To gain access to switches in row 2 proceed as follows:

1. Remove A6 switch assembly in accordance with paragraph 5-4(d)(3) and then referring to figure 5-43.

2. Remove screw 2 and nut through hole in switch frame connecting row 3 to mechanical linkage.

3. Remove screw and nut which is the 2 counter part at other end of row 3.

4. Remove screws 1, 3 and 4.

5. Row 3 of switches may now be "layed back" to gain access to row 2.

(d) To gain access to row 1 switches proceed as follows:

1. Remove row 1 as per paragraph 5-5a(4)(c).

2. Remove mechanical control between row 3 and row 2 near switches A6-S29 and S44.

Note

Be careful in replacing this part correctly; check function and position before removal.

3. Repeat procedure for row 2 removing the counter part screws and nuts.

(e) To reassemble proceed in the reverse order for removal.

CAUTION

Do not tighten screws and nuts (#2 for row 3, figure 5-43) connecting rows to linkage. Use glipthal or similar compound to hold nuts in place.

b. SPARE FUSES AND HOLDERS. - Each unit contains a spare fuse in the spare fuse holder. These fuses may be used to replace a blown fuse in that unit. The spare fuse holder may be used for a damaged active fuse holder on any unit.

c. AIR COOLING. - If it has been determined that a unit has or is failing due to external (room) high temperature, the unit may be pulled out in its extended locked position, with the top cover removed, and cooled by a external fan or blower. This may also be done if the fan of a unit has failed.

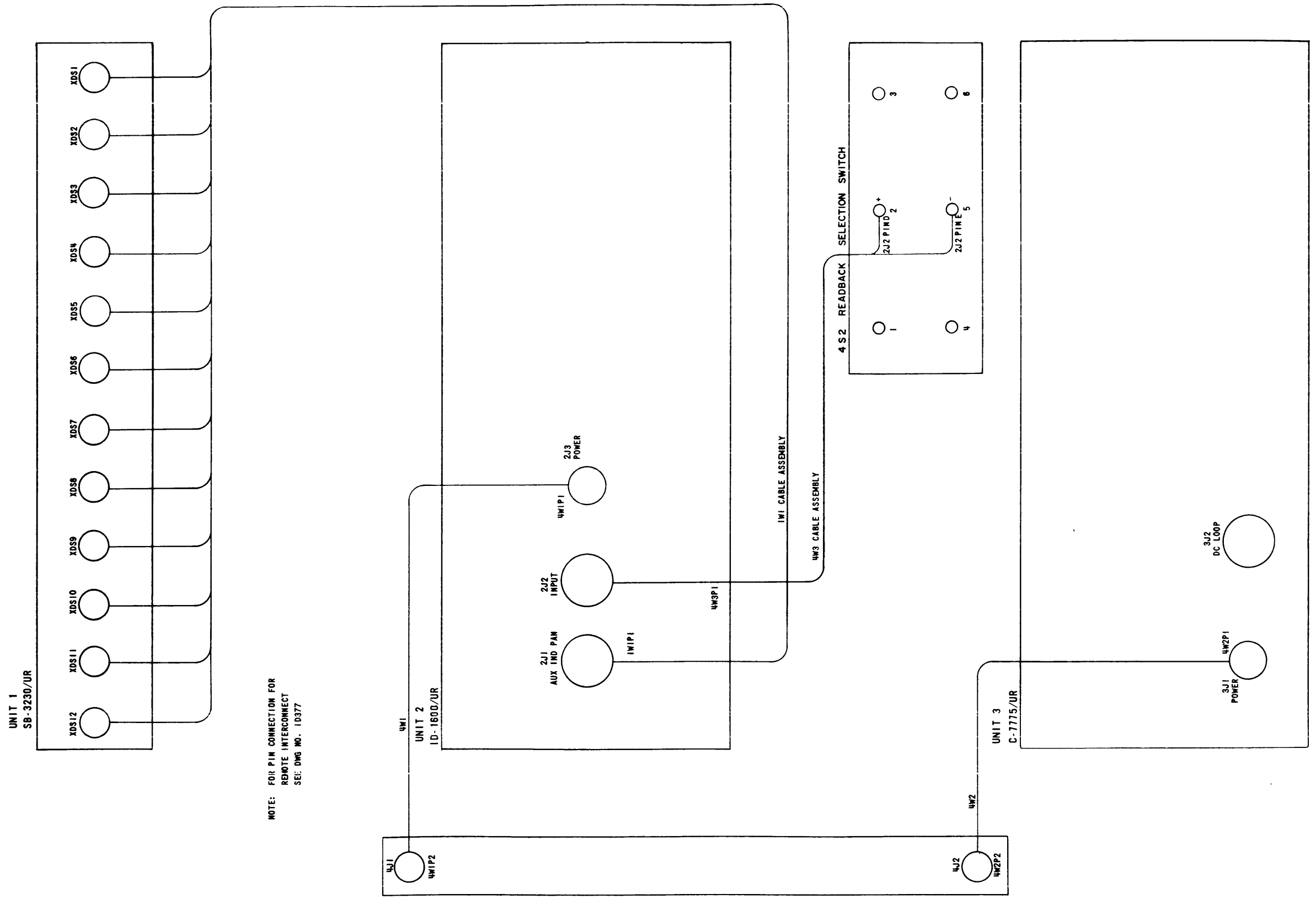
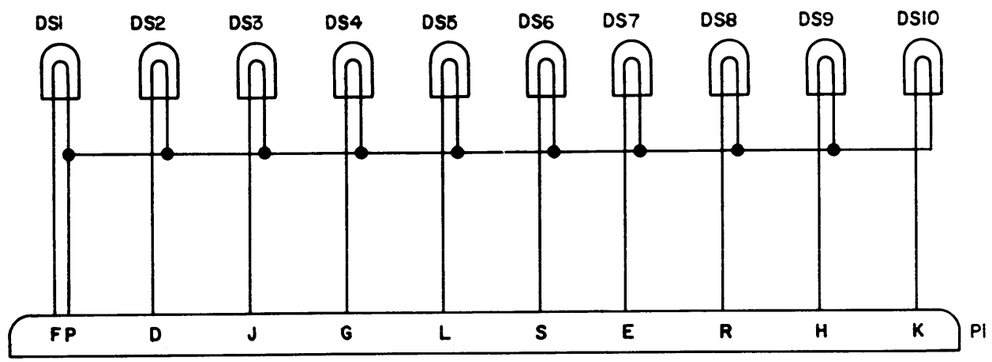


Figure 5-1. Rack Cabling Diagram, AN/URA-63



SYMBOLS	
LAST	MISSING
DS10 P1	

Figure 5-2. Schematic Diagram, SB-3230/UR

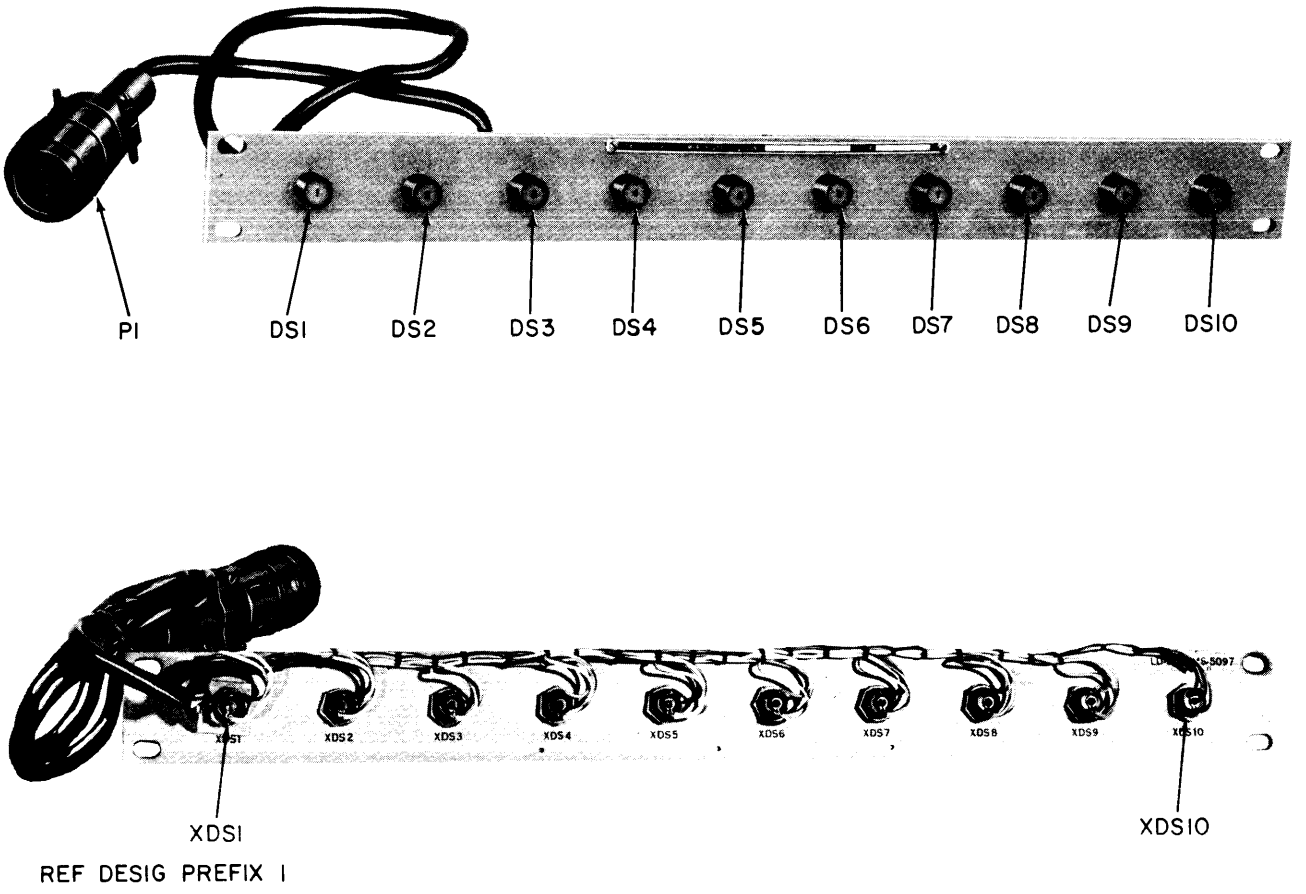


Figure 5-3. Component Locations, SB-3230/UR

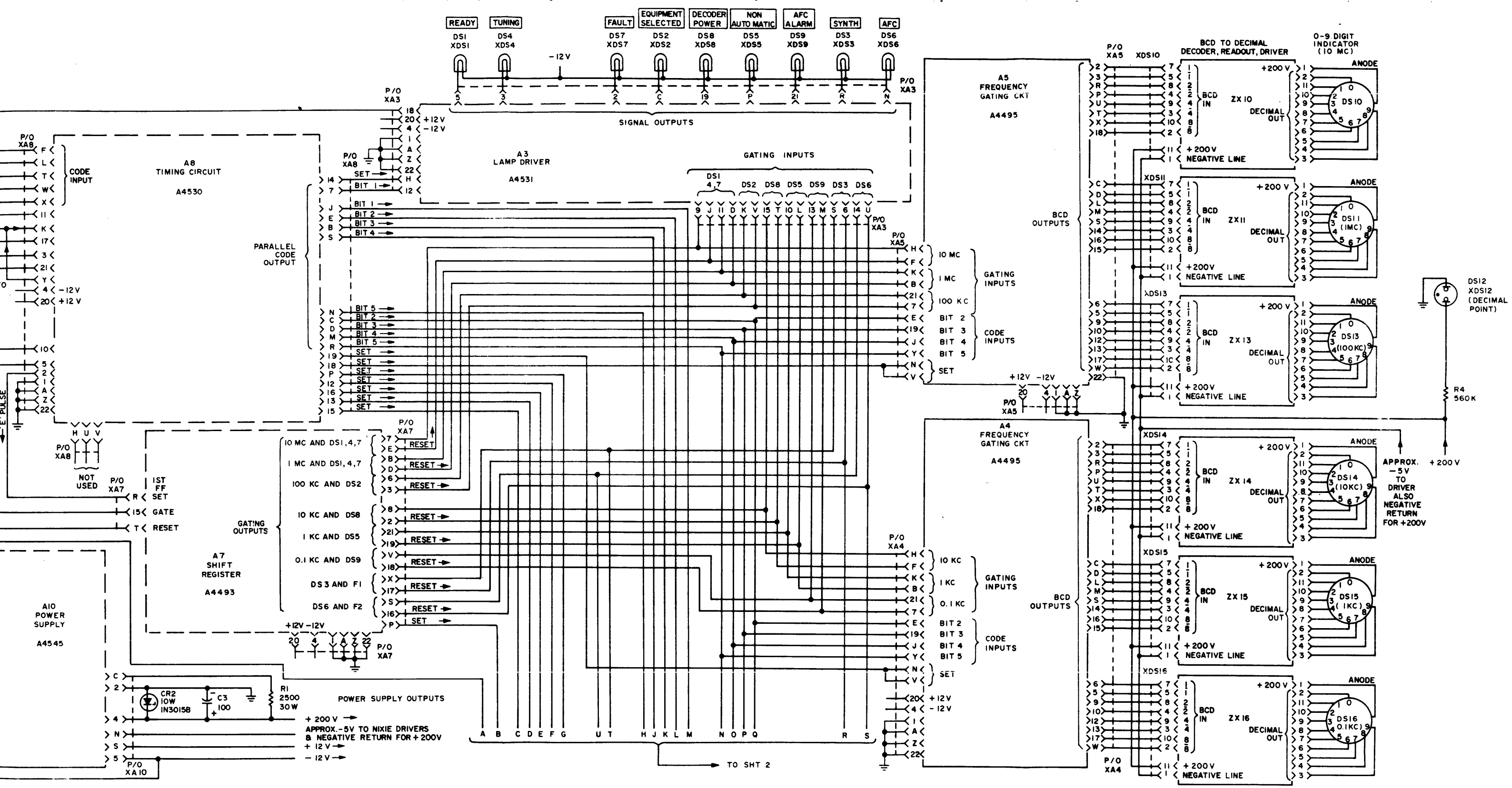
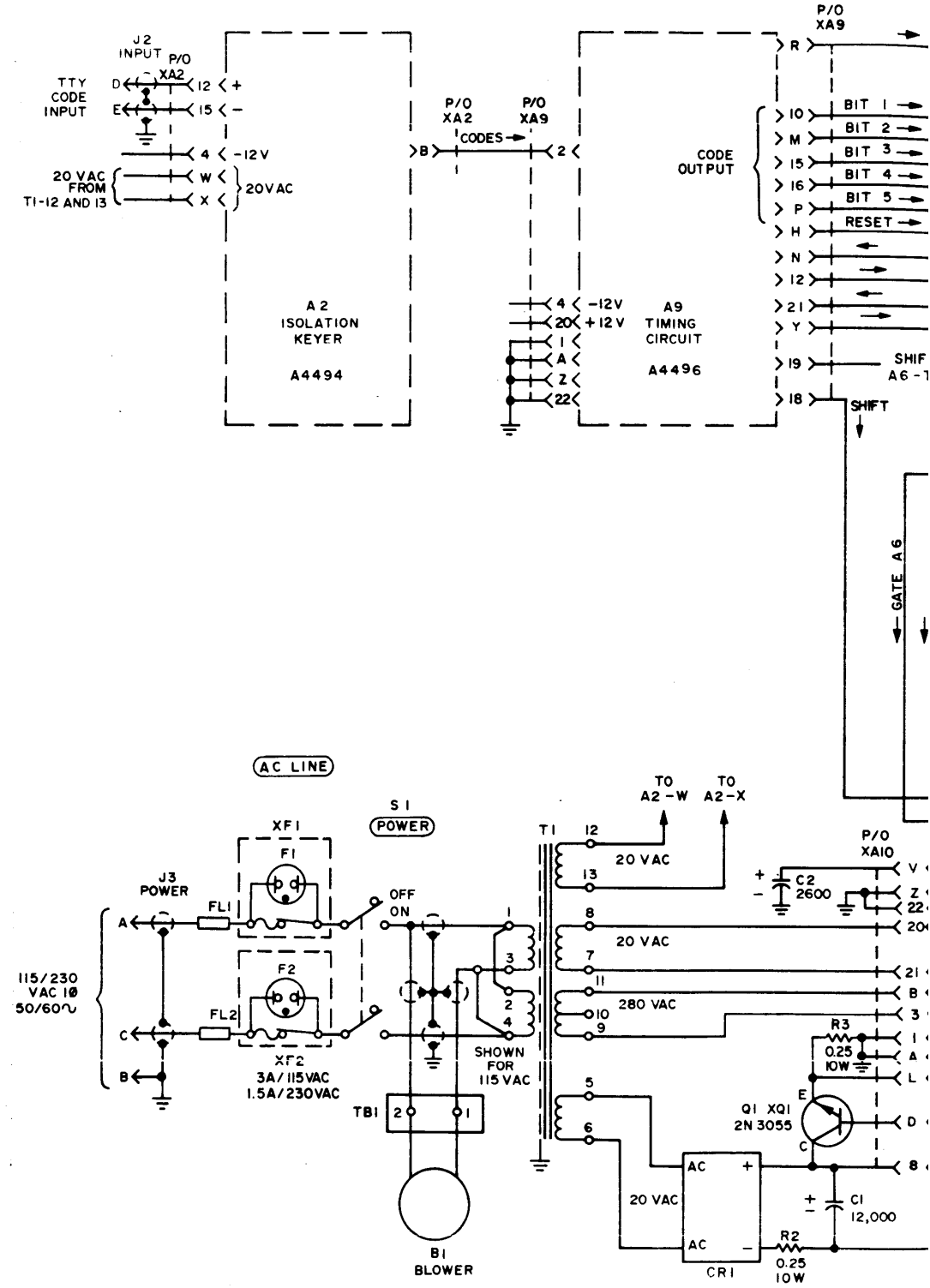


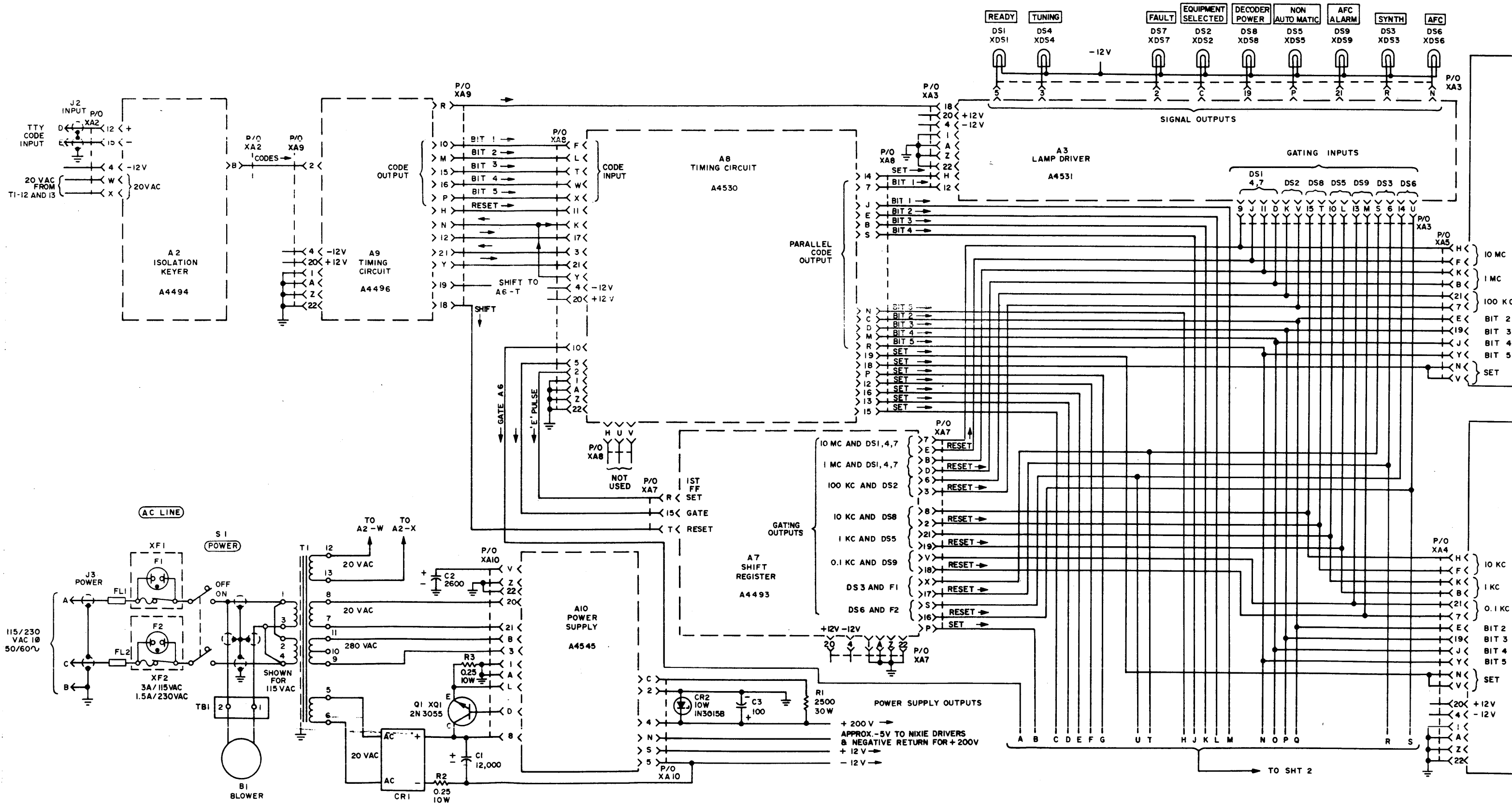
Figure 5-4. Interconnection Diagram, ID-1600/UR (Sheet 1 of 2)


J2 INPUT
P/O XA2
TTY CODE INPUT
D
E
12 +
15 −
4 −12V
20 VAC FROM T1-12 AND 13
W
X
20VAC
A2 ISOLATION KEYER
A4494
P/O XA2
P/O XA9
CODES
B
2
4 −12V
20 +12V
1
A
Z
22
A9 TIMING CIRCUIT
A4496
CODE OUTPUT
P/O XA9
R
10
M
15
16
P
H
N
12
21
Y
19
18
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
RESET
SHIFT
GATE A6
AC LINE
S1
POWER
XF1
F1
F2
XF2
3A/115VAC
1.5A/230VAC
J3 POWER
A
C
B
FL1
FL2
115/230 VAC 1Ø 50/60~
OFF ON
SHOWN FOR 115 VAC
TB1
B1 BLOWER
T1
12
13
20 VAC
8
7
11
10
9
280 VAC
5
6
TO A2-W
TO A2-X
P/O XA10
C2 2600
R3 0.25 10W
Q1 XQ1 2N3055
E
C
C1 12,000
R2 0.25 10W
AC
CR1

ORIGINAL

NAVELEX 0967-385-1010

NAVELEX 0967-385-1010



NAVELEX 0967-385-1010

Figure 5-4

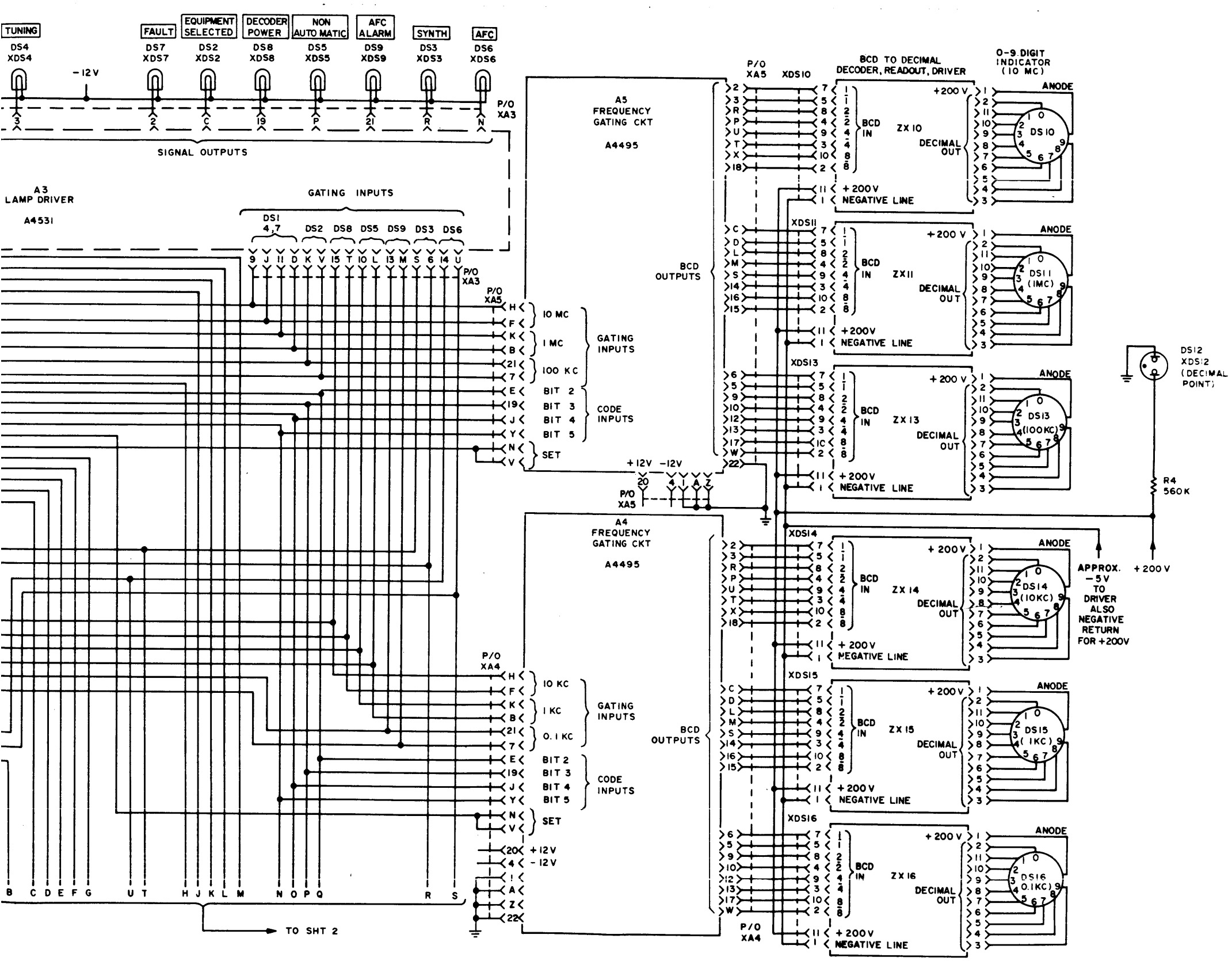


Figure 5-4. Interconnection Diagram, ID-1600/UR (Sheet 1 of 2)

NAVELEX 0967-385-1010

NAVELEX 0967-385-1010

TABLE "A" READOUT FUNCTIONS (ID-1600/UR)

READOUT FUNCTION	REFERENCE SYMBOL	POS TYPE	TMC P/N	DS PANEL MARKING
10	A1	12	A4492	
9	A11	NONE		
8	A12	NONE		
7	A13	NONE		
6	A14	DUAL-4	A4625	
5	A15	DUAL-4	A4625	
4	A16	12	A4492	
3	A17	NONE		
2	A18	NONE		
1	A19	NONE		
1	DS17	NONE		
2	DS18	NONE		
3	DS19	NONE		
4	DS20	12	IC 105-2	MODE
5	DS21	DUAL-4	IC 105-1	AGC TIME CONSTANT, SYM/B2, B1
6	DS22	DUAL-4	IC 105-1	AGC TIME CONSTANT, A2-A1
7	DS23	NONE		
8	DS24	NONE		
9	DS25	NONE		

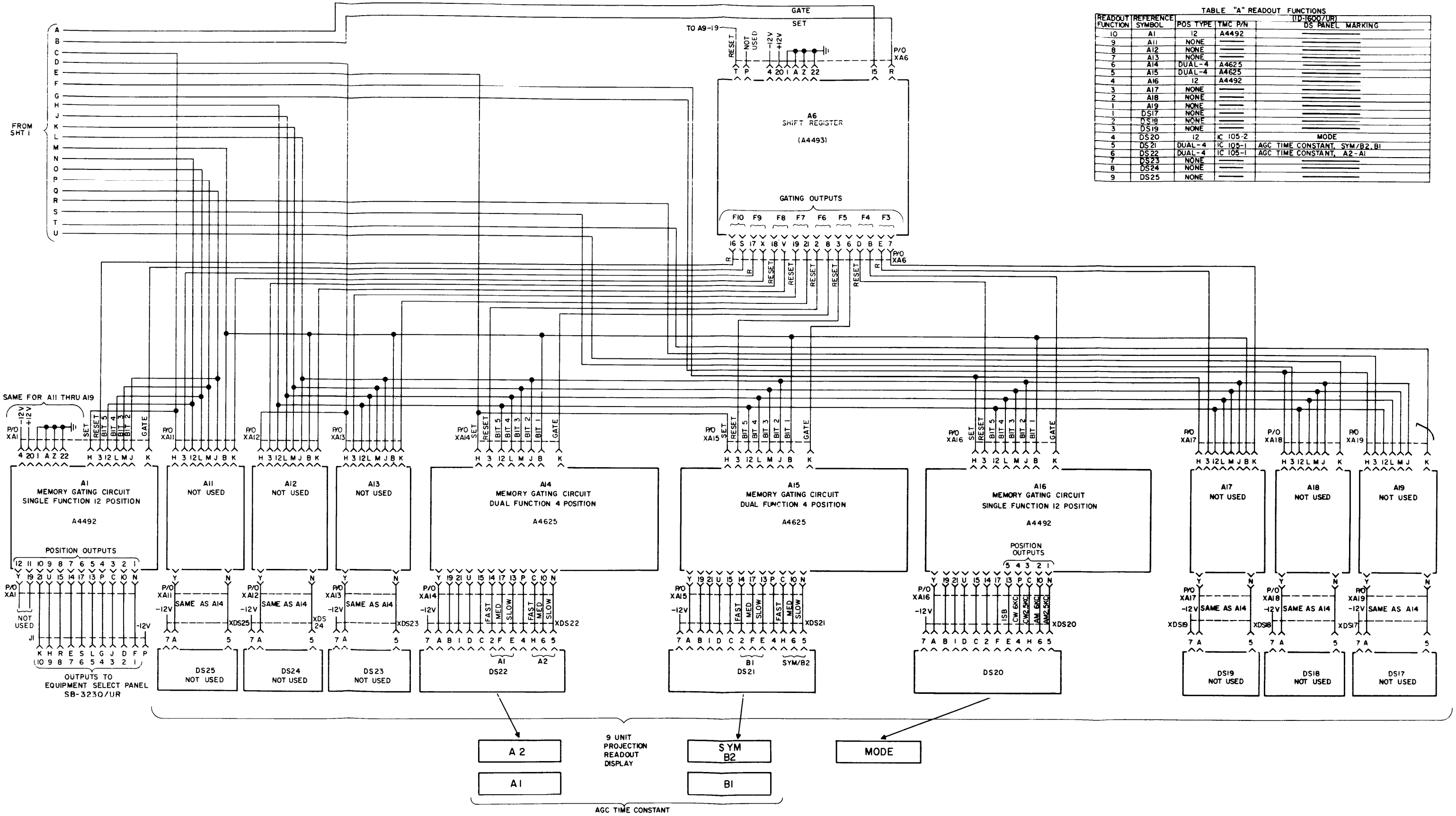
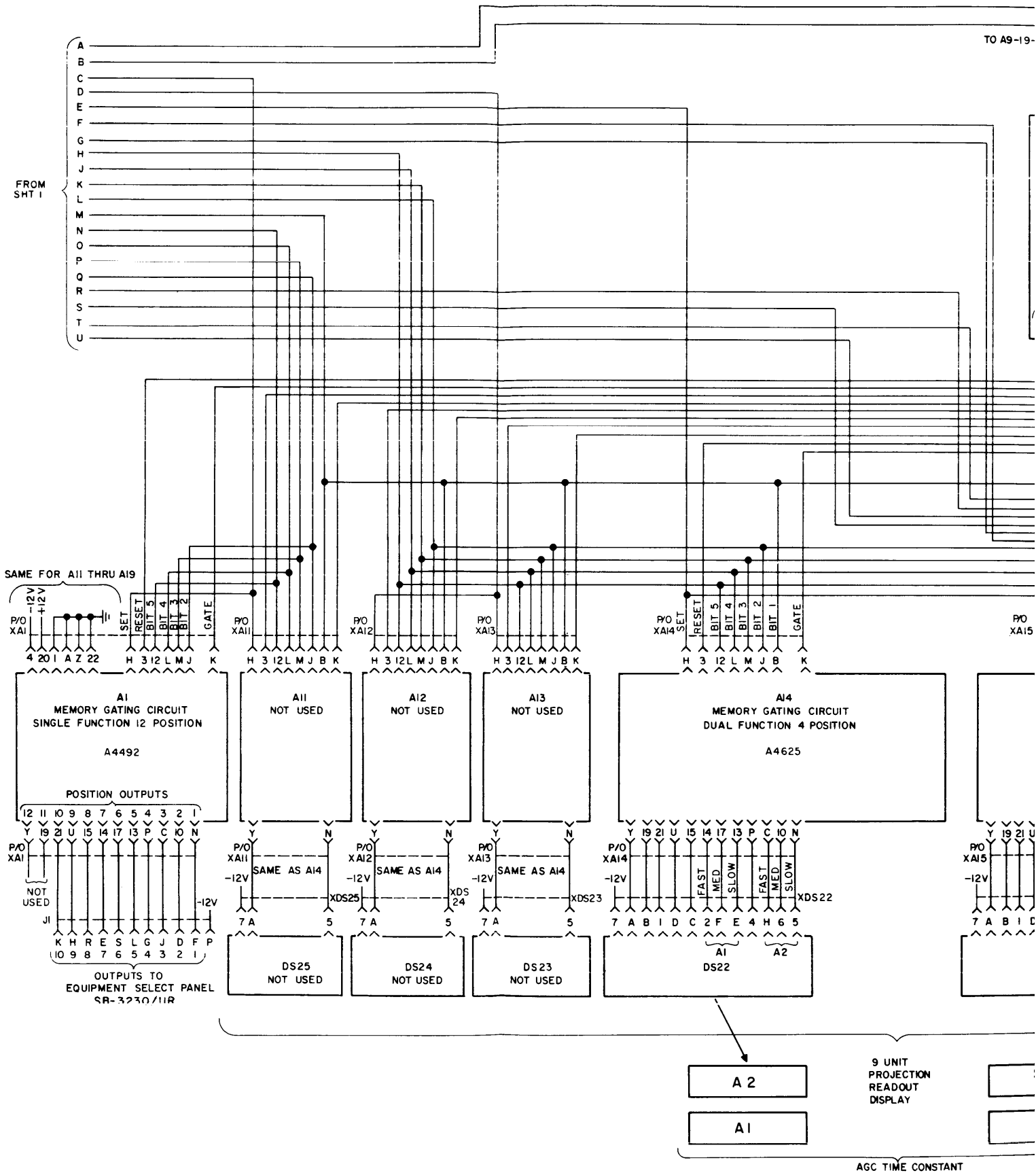


Figure 5-4. Interconnection Diagram, ID-1600/UR (Sheet 2 of 2)



NOTES:
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION AS APPLICABLE
2. LAST SYMBOLS USED; A19, C3, CR2, DS25, F2, FL2, J3, Q1, S1, T1, TB1, XA19, XDS25, ZX16, XQ1, R4, B1
3. MISSING SYMBOLS: ZX1 THRU ZX9, & ZX12
4. UNLESS OTHERWISE SPECIFIED: ALL RESISTOR VALUES ARE IN OHMS, ALL CAPACITOR VALUES ARE IN MICROFARADS.
5. USAGE OF PLUG-IN ASSEMBLIES A1, A11 THRU A19 AND DS17 THRU DS25 WILL VARY. REFER TO TABLE "A"

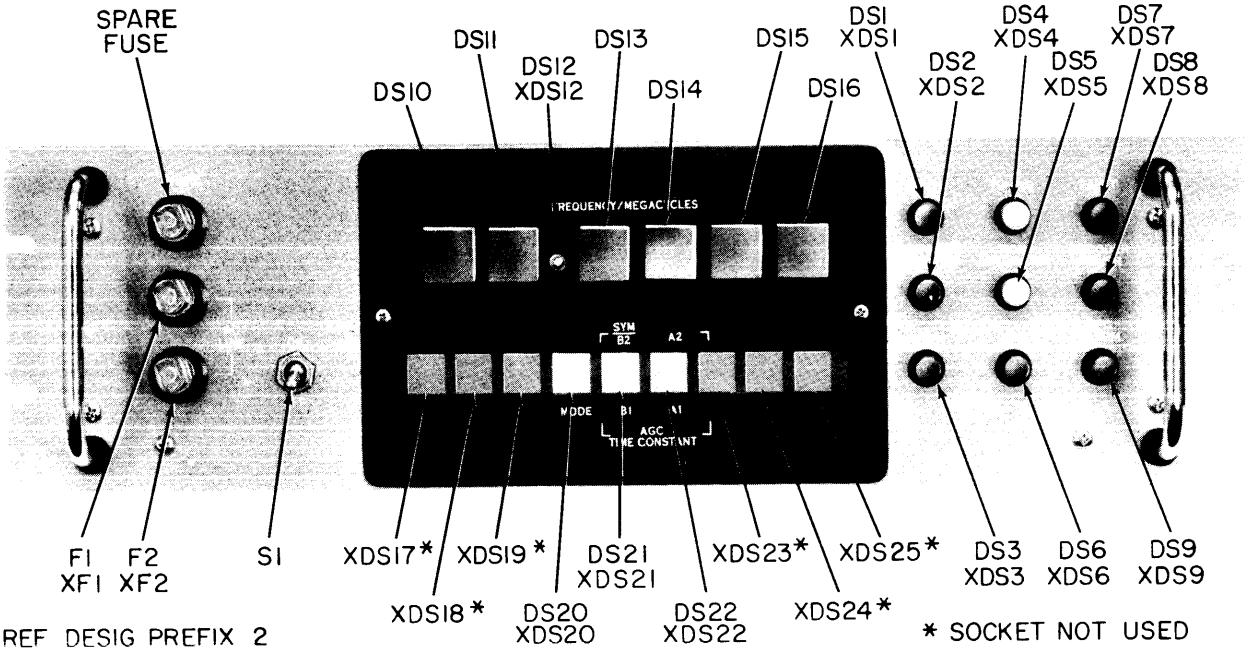


Figure 5-5. Major Component Locations, Front Panel of ID-1600/UR

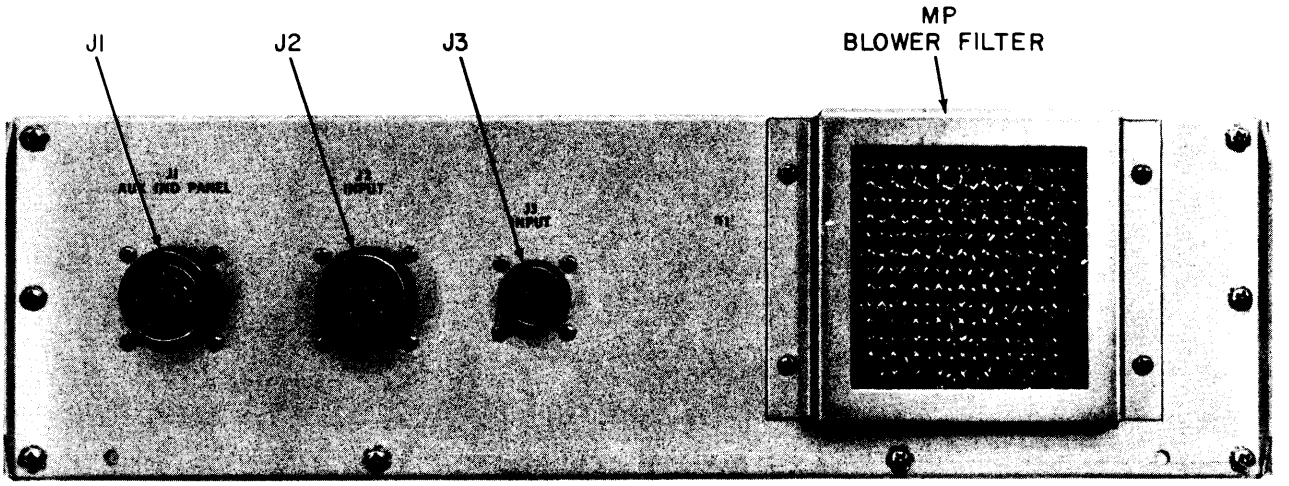


Figure 5-6. Major Component Locations,
Rear Panel of ID-1600/UR

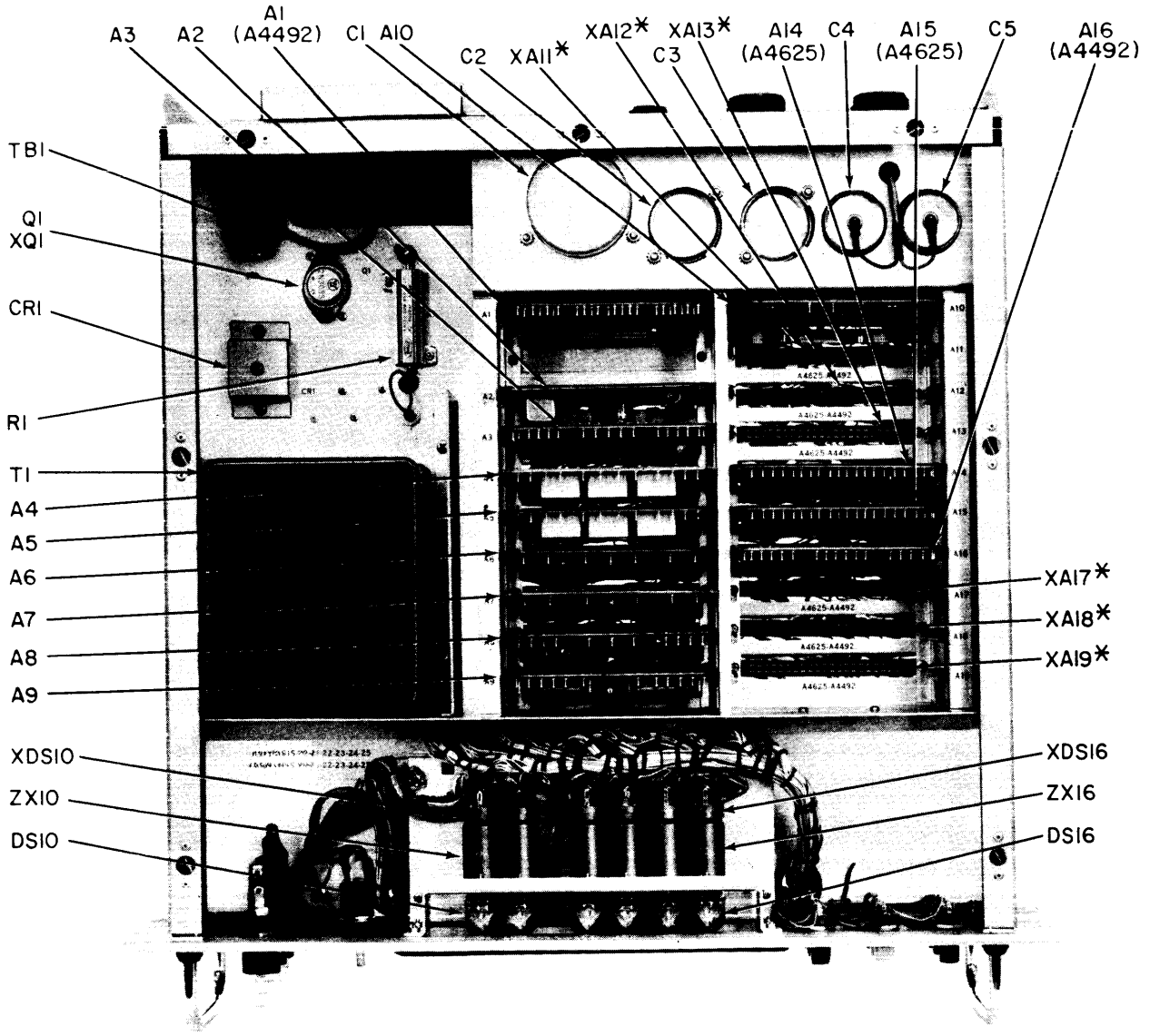


Figure 5-7. Major Component Locations
Top View of ID-1600/UR

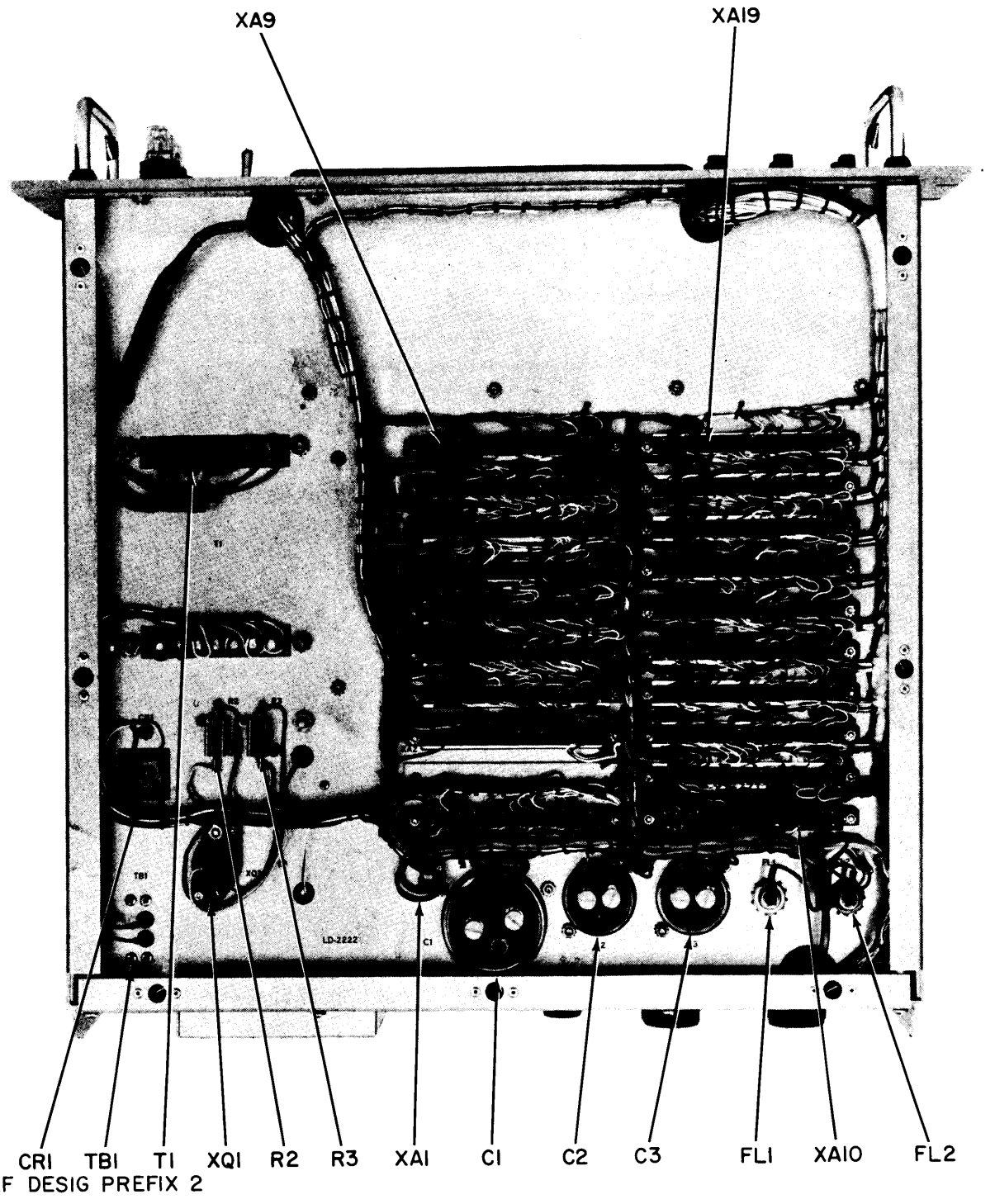
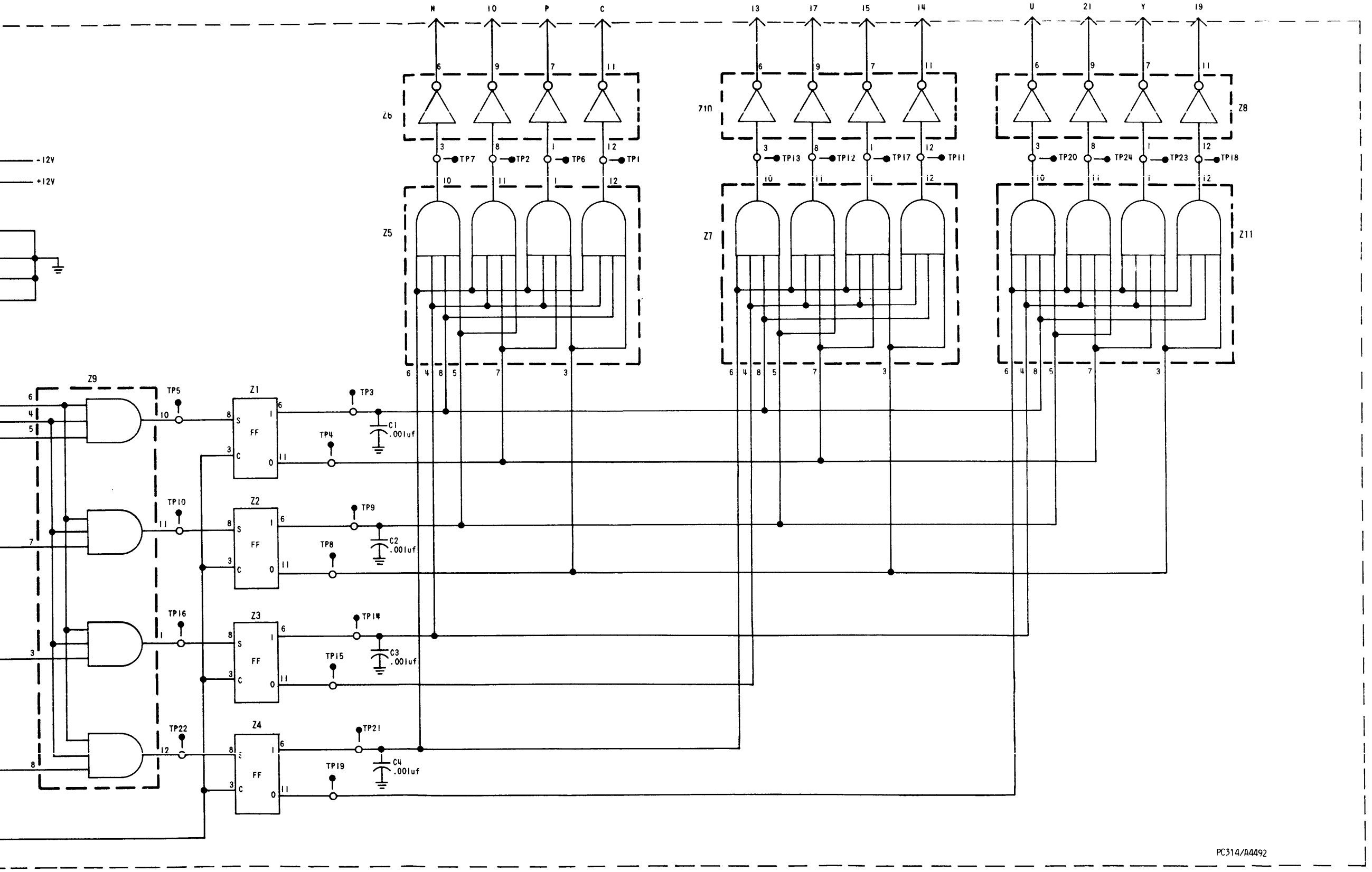


Figure 5-8. Major Component Locations,
Bottom View of ID-1600/UR



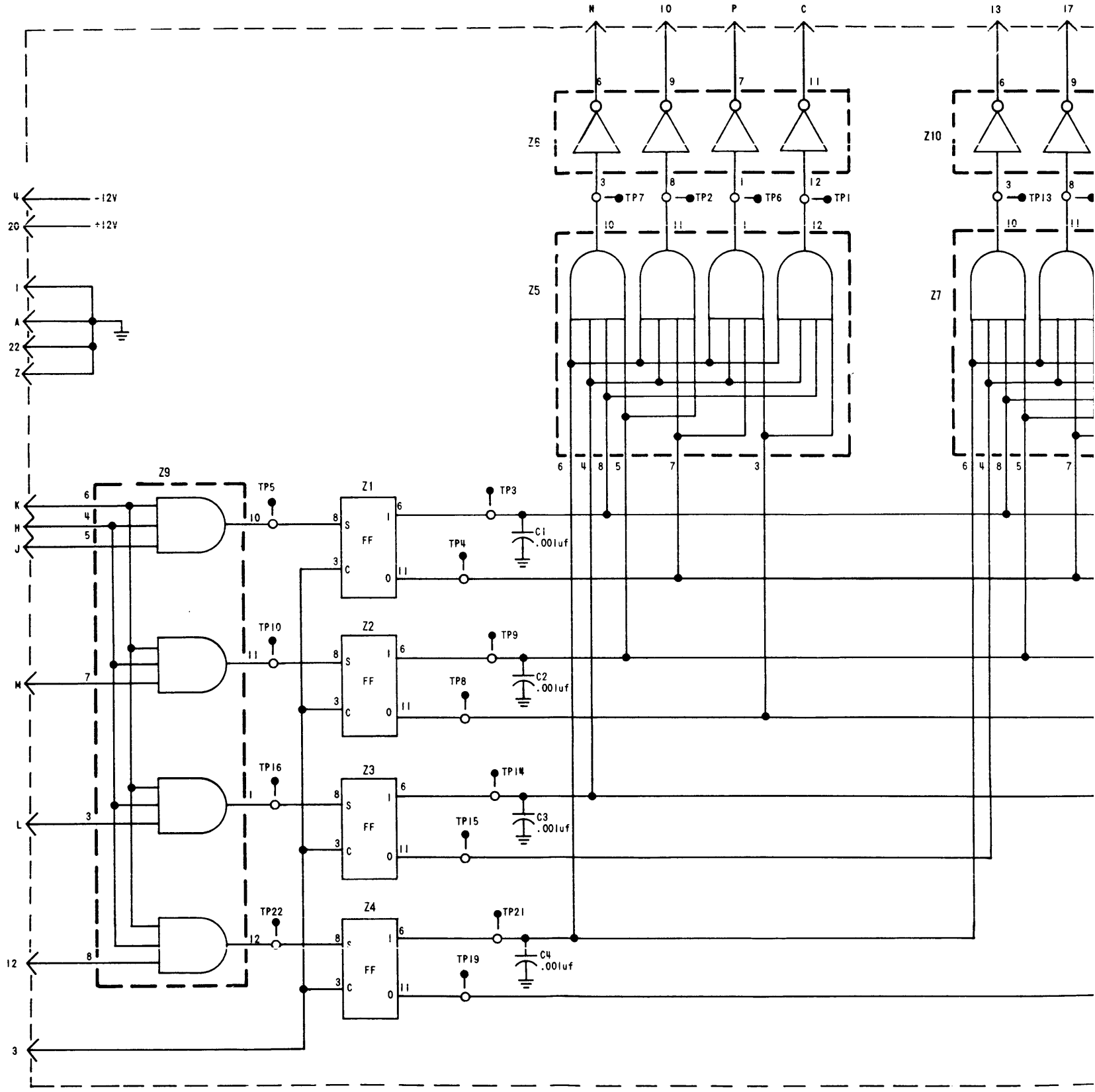
LAST SYMBOL	MISSING SYMBOL
C4 TP24 Z11	

MODULE VOLTAGE AND GND CHART			
	PIN CONNECTIONS		
SYMBOL	+12V	-12V	GND
Z1 THRU Z4	10	2	5
Z5,Z7,Z9,Z11		2	
Z6,Z8,Z10	10		5

NOTE:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE

Figure 5-9. Memory/Gating Circuits 2A1 and 2A16, Schematic Diagram


N
10
P
C
13
17
Z6
Z10
Z5
Z7
Z9
Z1
Z2
Z3
Z4
-12V
+12V
TP7
TP2
TP6
TP1
TP13
TP5
TP3
TP4
TP10
TP9
TP8
TP16
TP14
TP15
TP22
TP21
TP19
C1 .001uf
C2 .001uf
C3 .001uf
C4 .001uf
FF
K
H
J
M
L

ORIGINAL

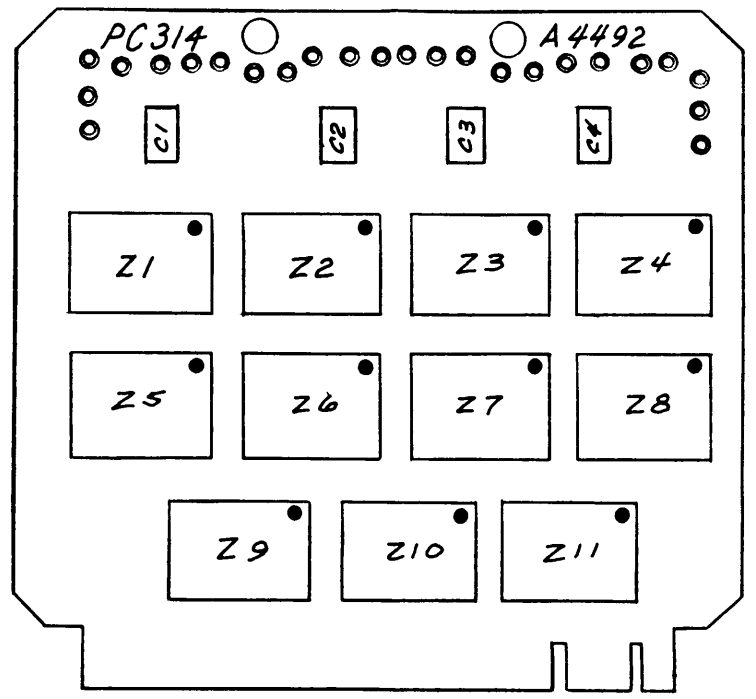
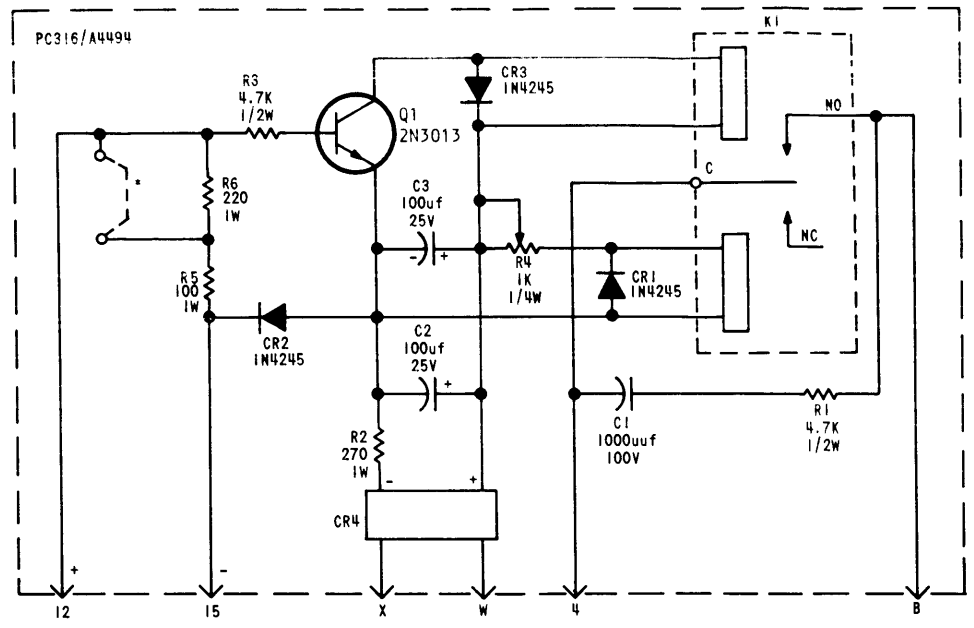


Figure 5-10. Memory/Gating Circuits 2A1 and 2A16, Component Locations



LAST SYMBOL	MISSING SYMBOL
R6 C3 CR4 K1 Q1	

NOTES

1. PARTIAL REFERENCE DESIGNATIONS AS SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION (S) AS APPLICABLE
* 2. STRAP IS INCLUDED WHEN 60mA LOOP IS USED STRAP IS NOT INCLUDED WHEN 20mA OR 6 VOLT LOOPS ARE USED.

Figure 5-11. Isolation Keyer 2A2, Schematic Diagram

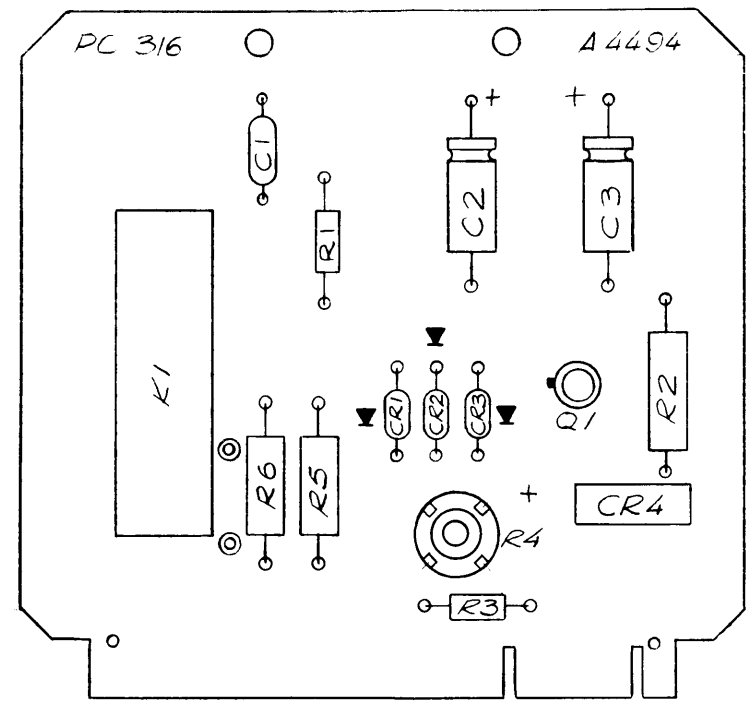
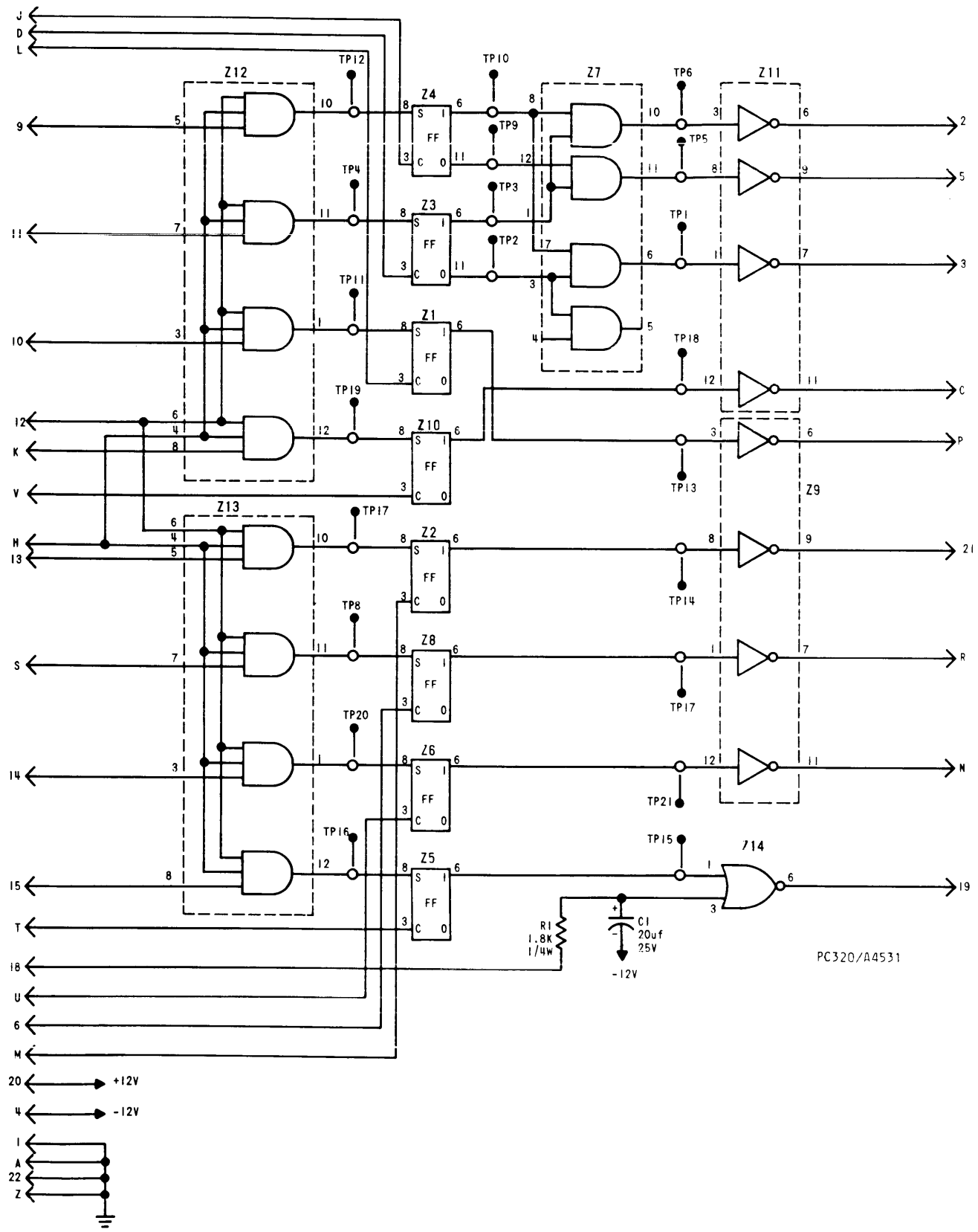


Figure 5-12. Isolation Keyer 2A2,
Component Locations



MODULE VOLTAGE AND GND CHART

SYMBOL	PIN CONNECTIONS		
	+12	-12V	GND
Z1 THRU Z6, Z8, Z10	10	2	5
Z7, Z11 THRU Z13		2	
Z9, Z14	10		5

LAST SYMBOL	MISSING SYMBOL
C1 R1 TP21 Z14	

NOTE:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE

Figure 5-13. Lamp Driver 2A3, Schematic Diagram

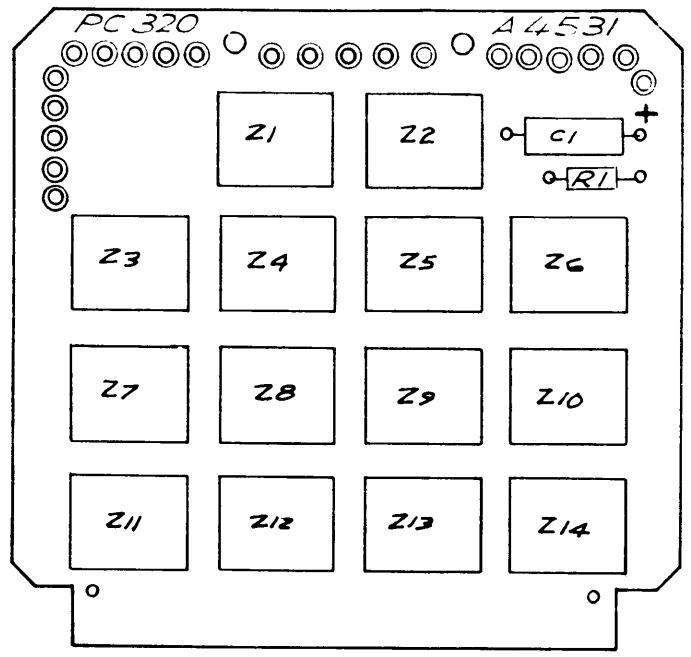
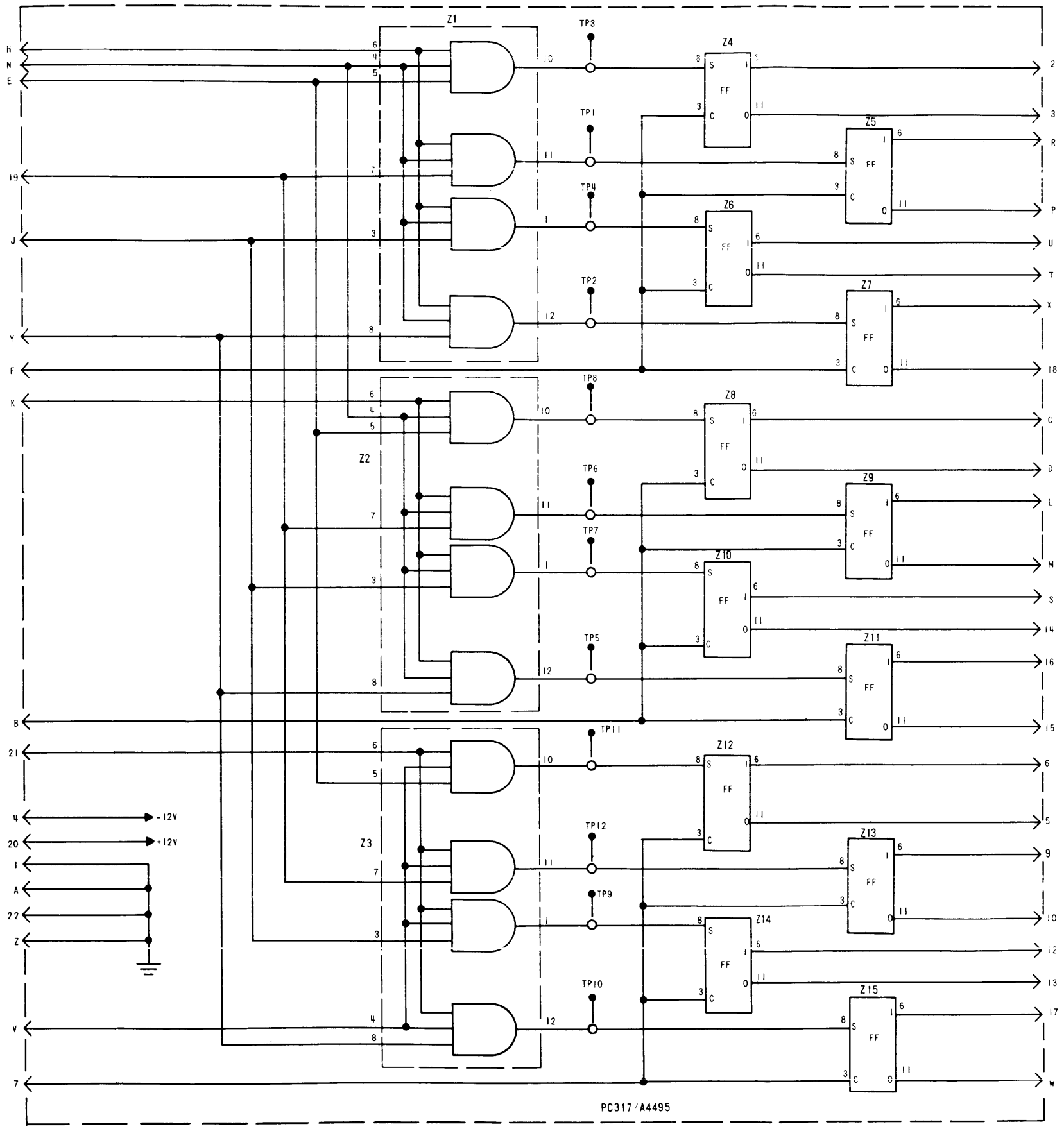


Figure 5-14. Lamp Driver 2A3,
Component Locations

NAVELEX 0967-385-1010



MODULE VOLTAGE & GND CHART			
SYMBOL	PIN CONNECTIONS		
	+12V	-12V	GND
Z1, Z2, Z3		2	
Z4 THRU Z15	10	2	5

LAST SYMBOL	MISSING SYMBOL
TP12 Z15	

NOTE:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE

Figure 5-15. Frequency Gating Circuit, 2A4 and 2A5, Schematic Diagram

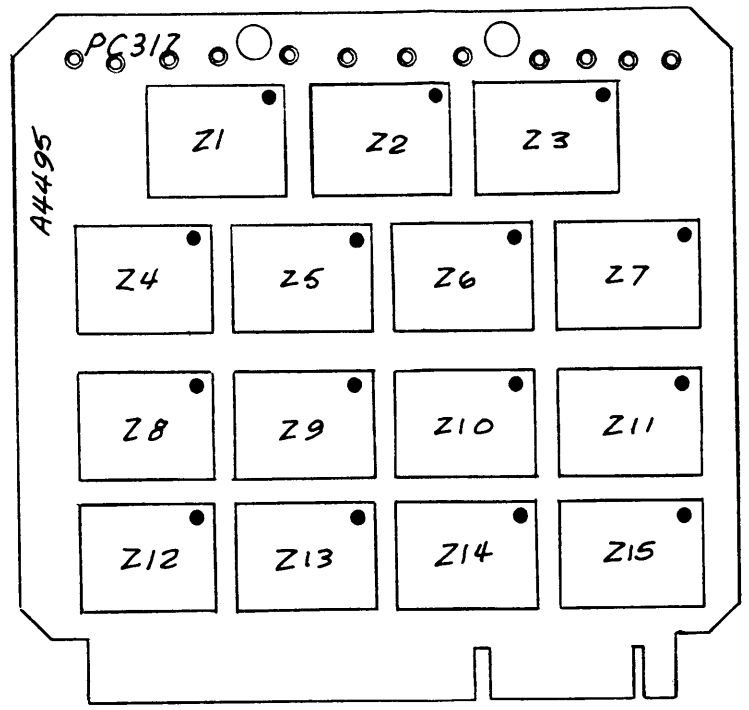
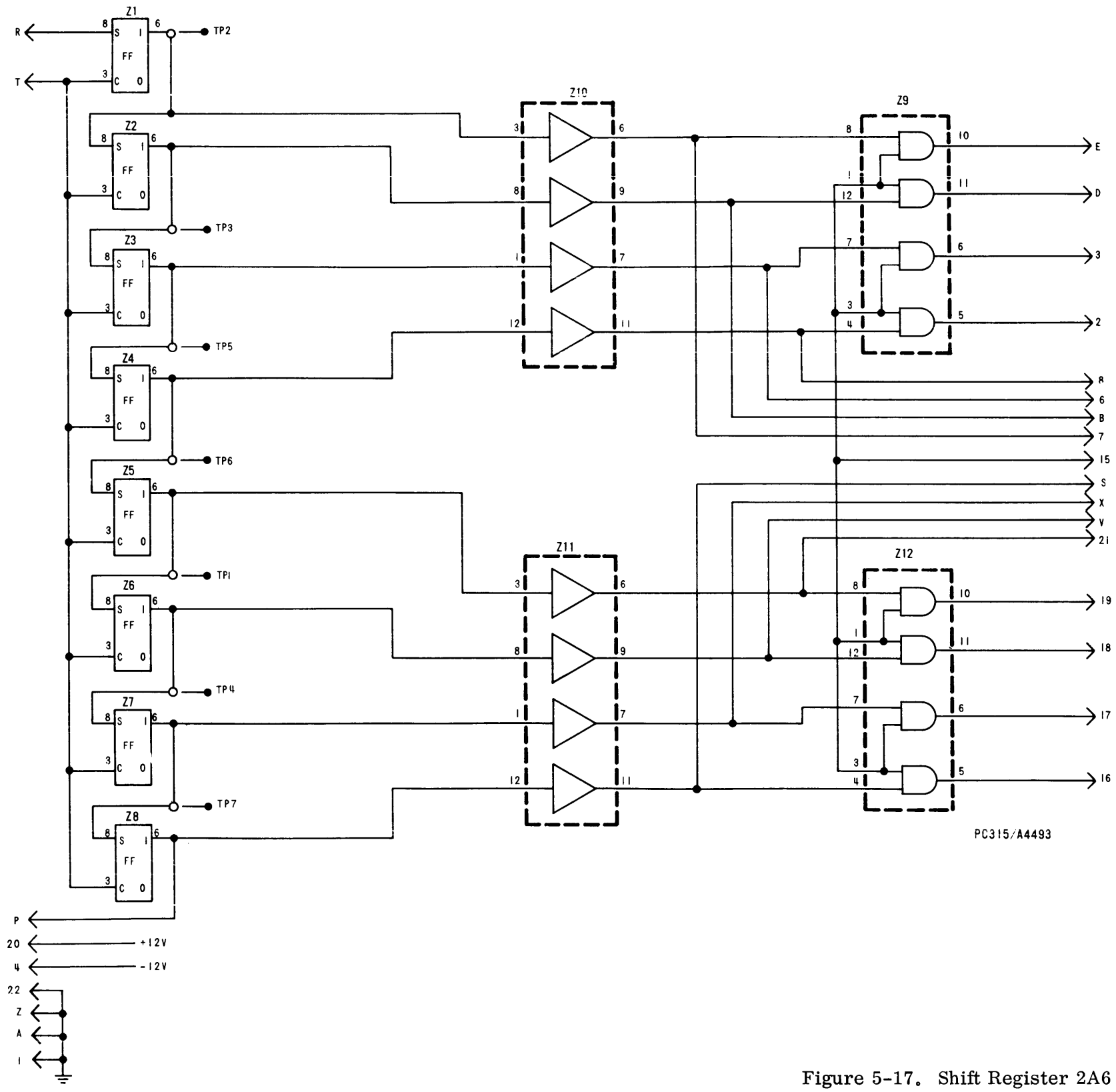


Figure 5-16. Frequency Gating Circuit, 2A4 and 2A5, Component Locations

NAVELEX 0967-385-1010



MODULE VOLTAGE & GND CHART			
SYMBOL	PIN CONNECTIONS		
	+12V	-12V	GND
Z1 THRU Z8	10	2	5
Z9, Z12		2	
Z10, Z11		2	5

LAST SYMBOL	MISSING SYMBOL
TP7 Z12	

NOTE:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE.

Figure 5-17. Shift Register 2A6 and 2A7, Schematic Diagram

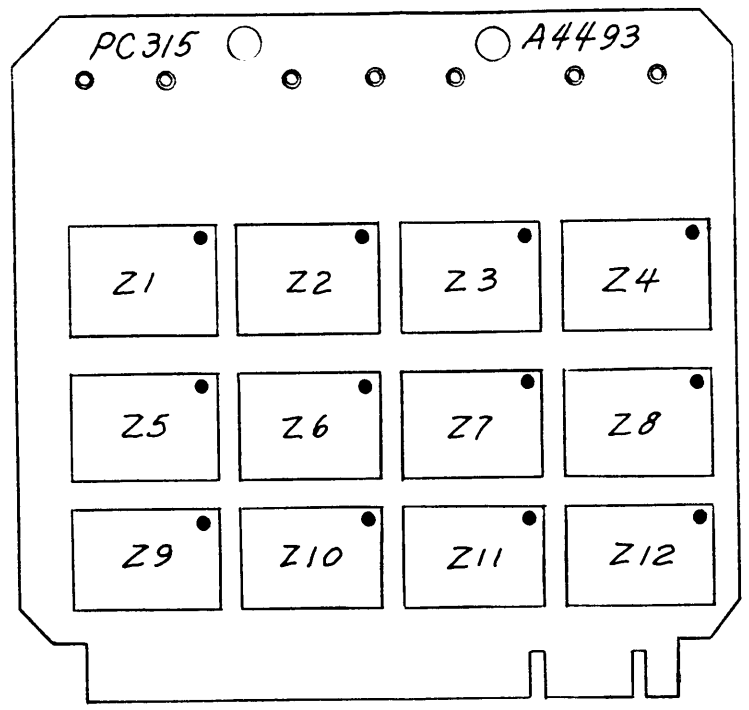
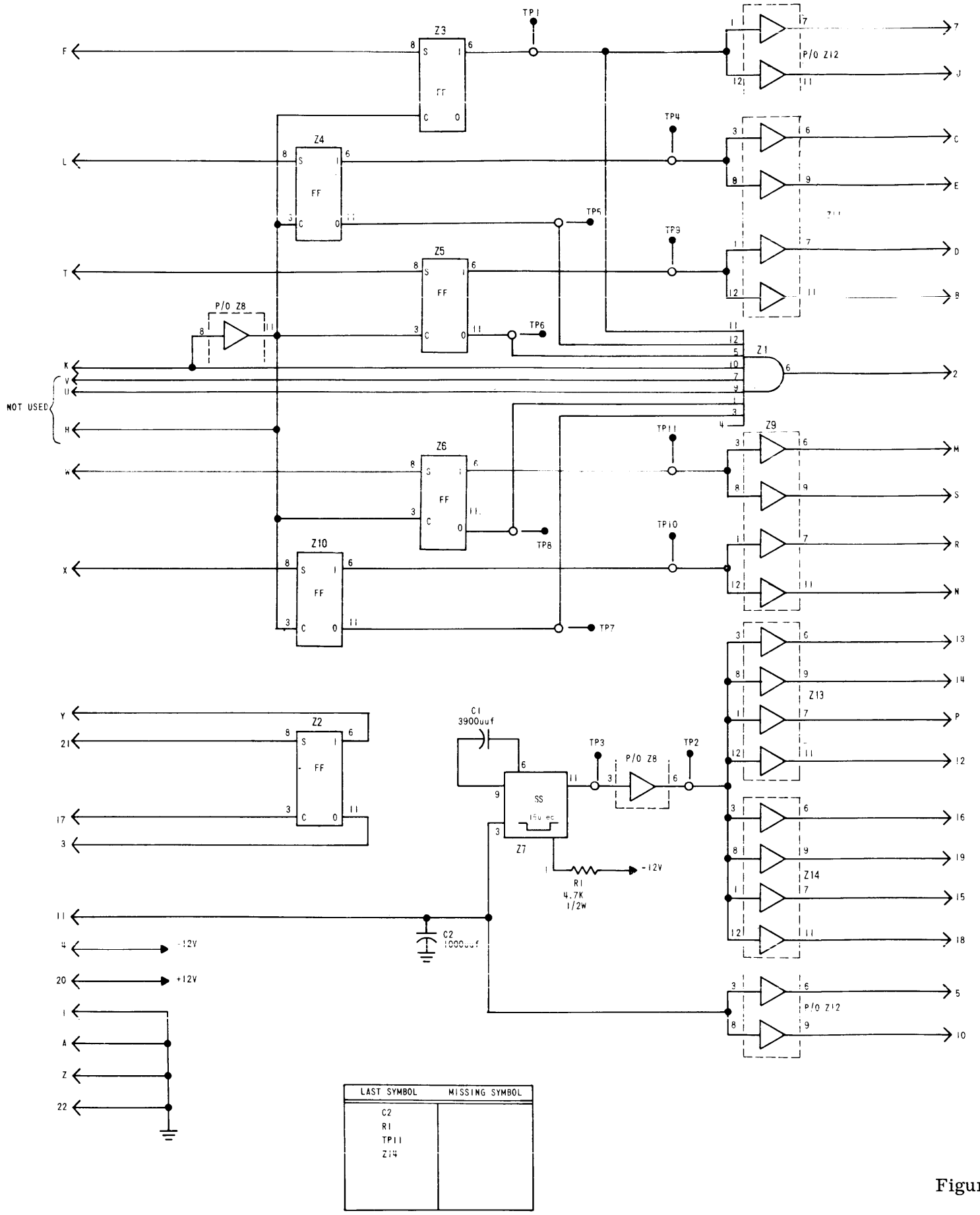


Figure 5-18. Shift Register 2A6 and 2A7
Component Locations

NAVELEX 0967-385-1010



MODULE VOLTAGE AND GND CHART			
	PIN CONNECTIONS		
SYMBOL	+12V	-12V	GND
Z1		2	
Z1 THRU Z7,Z10	10	2	5
Z8,Z9,Z11 THRU Z14		2	5

NOTE:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE

LAST SYMBOL	MISSING SYMBOL
C2	
R1	
TP11	
Z14	

Figure 5-19. Timing Circuit 2A8, Schematic Diagram

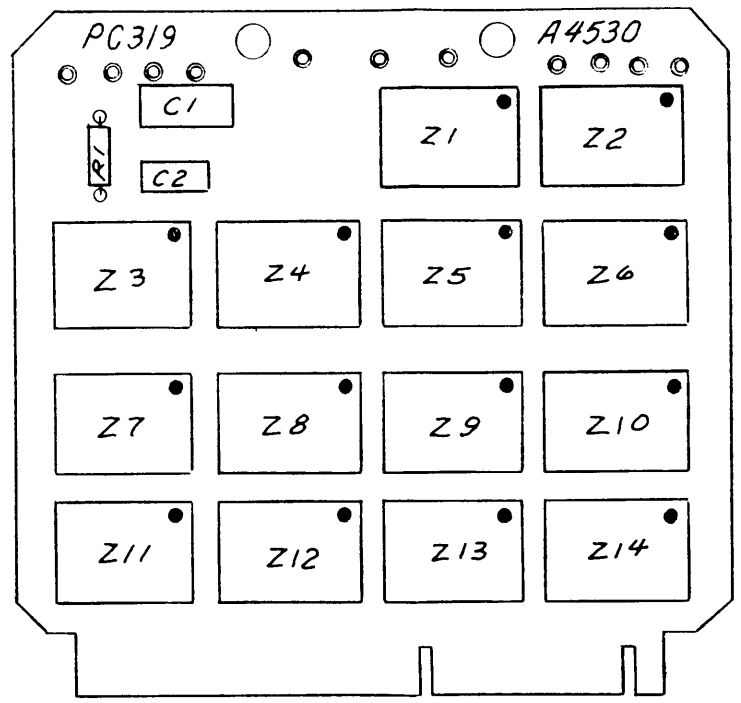


Figure 5-20. Timing Circuit 2A8,
Component Locations

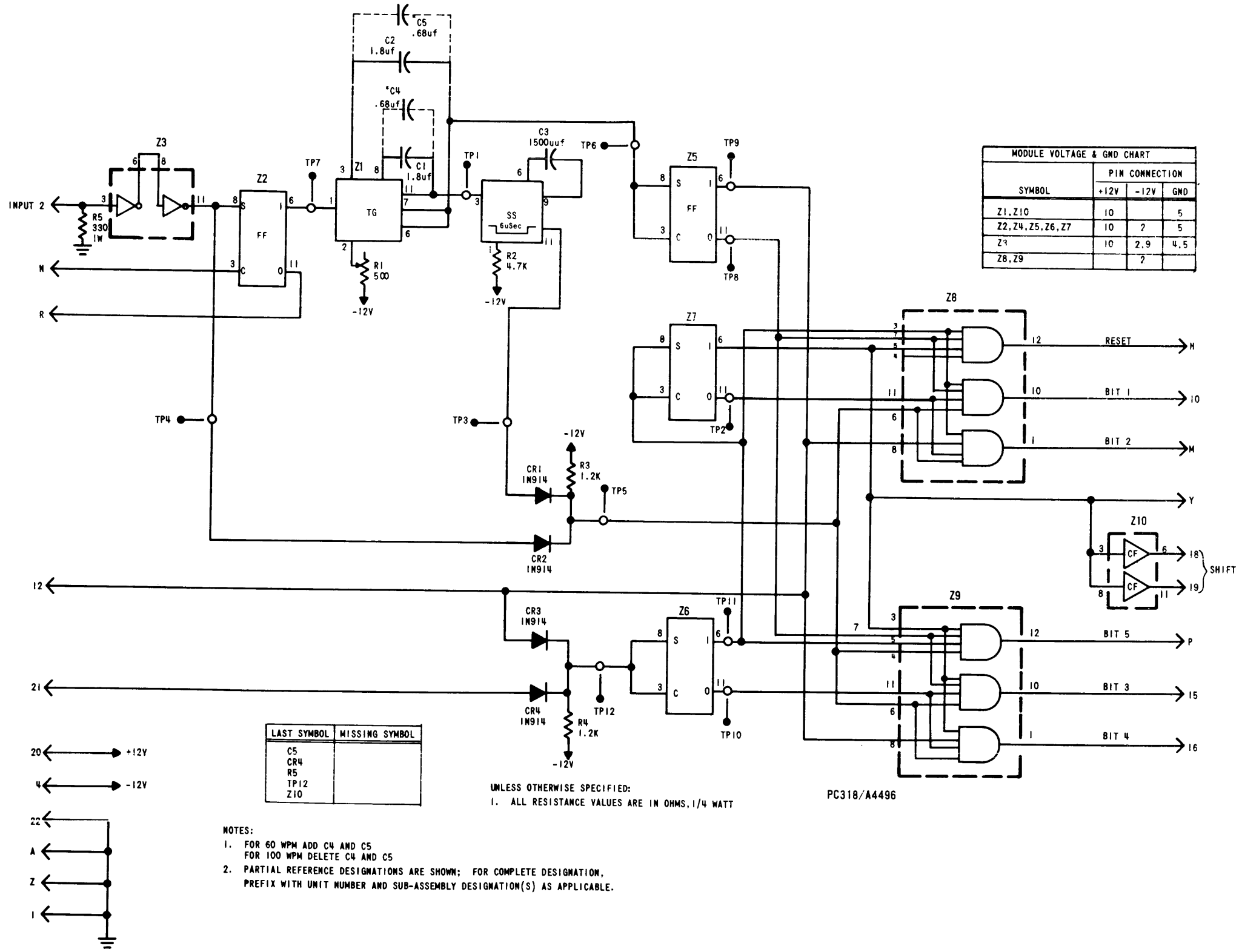


Figure 5-21. Timing Circuit 2A9, Schematic Diagram

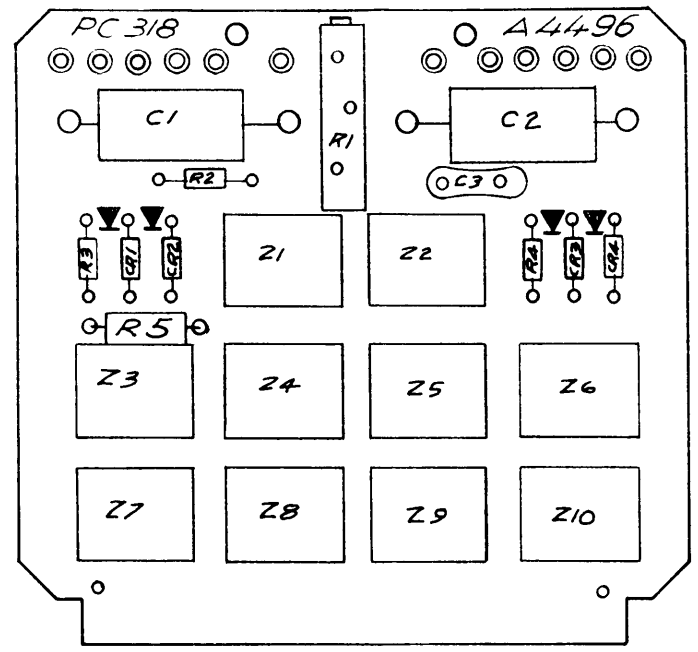
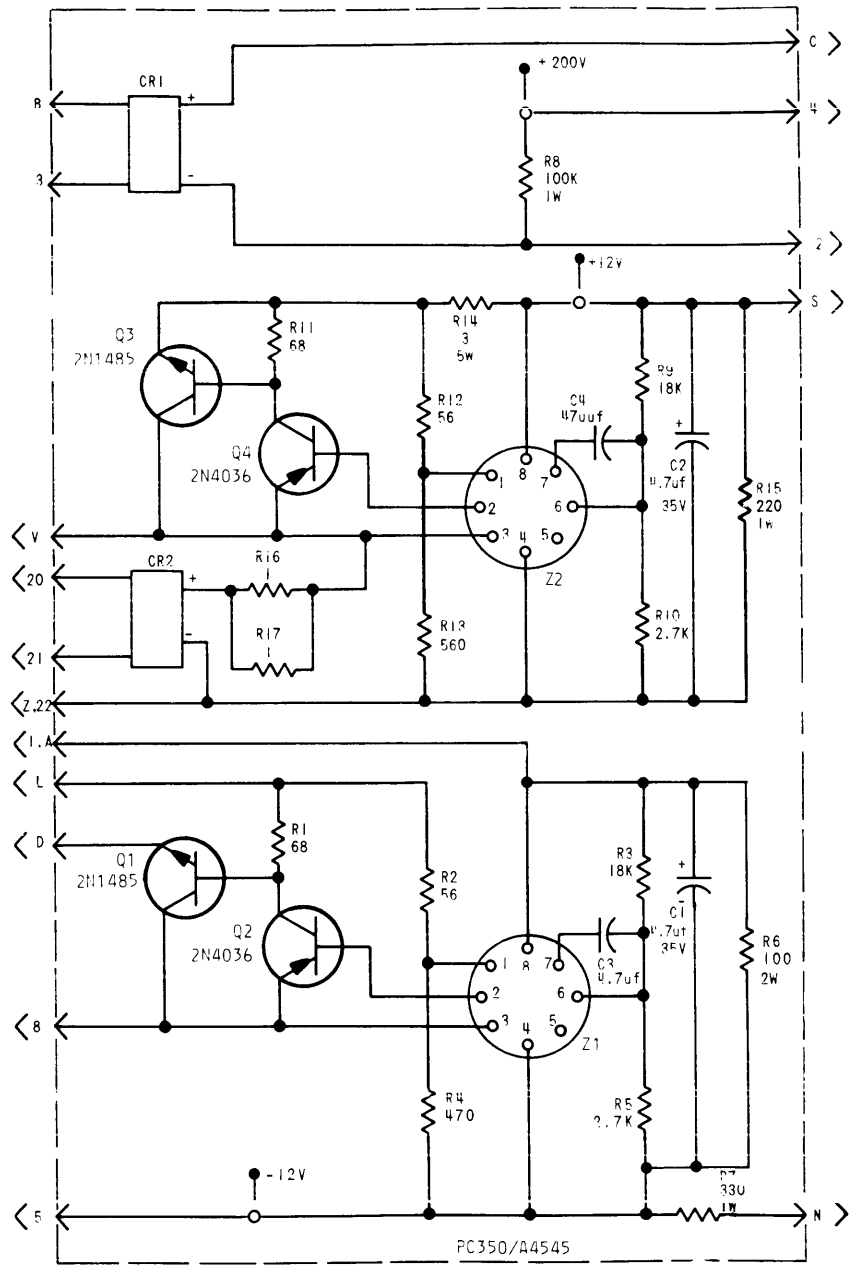


Figure 5-22. Timing Circuit 2A9,
Component Locations



LAST SYMBOL	MISSING SYMBOL
C4	
CR2	
Q4	
R17	
Z2	

UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTANCE VALUES ARE IN OHMS, 1/2 WATT
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE

Figure 5-23. Power Supply 2A10, Schematic Diagram

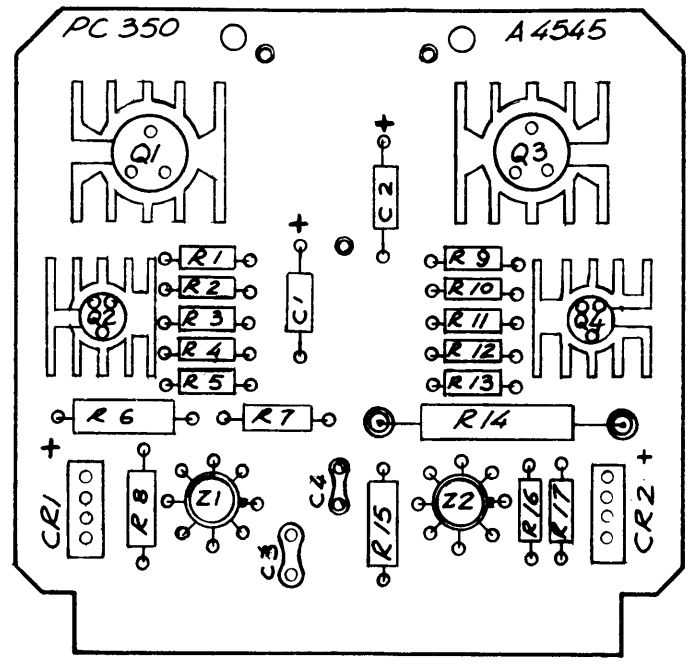
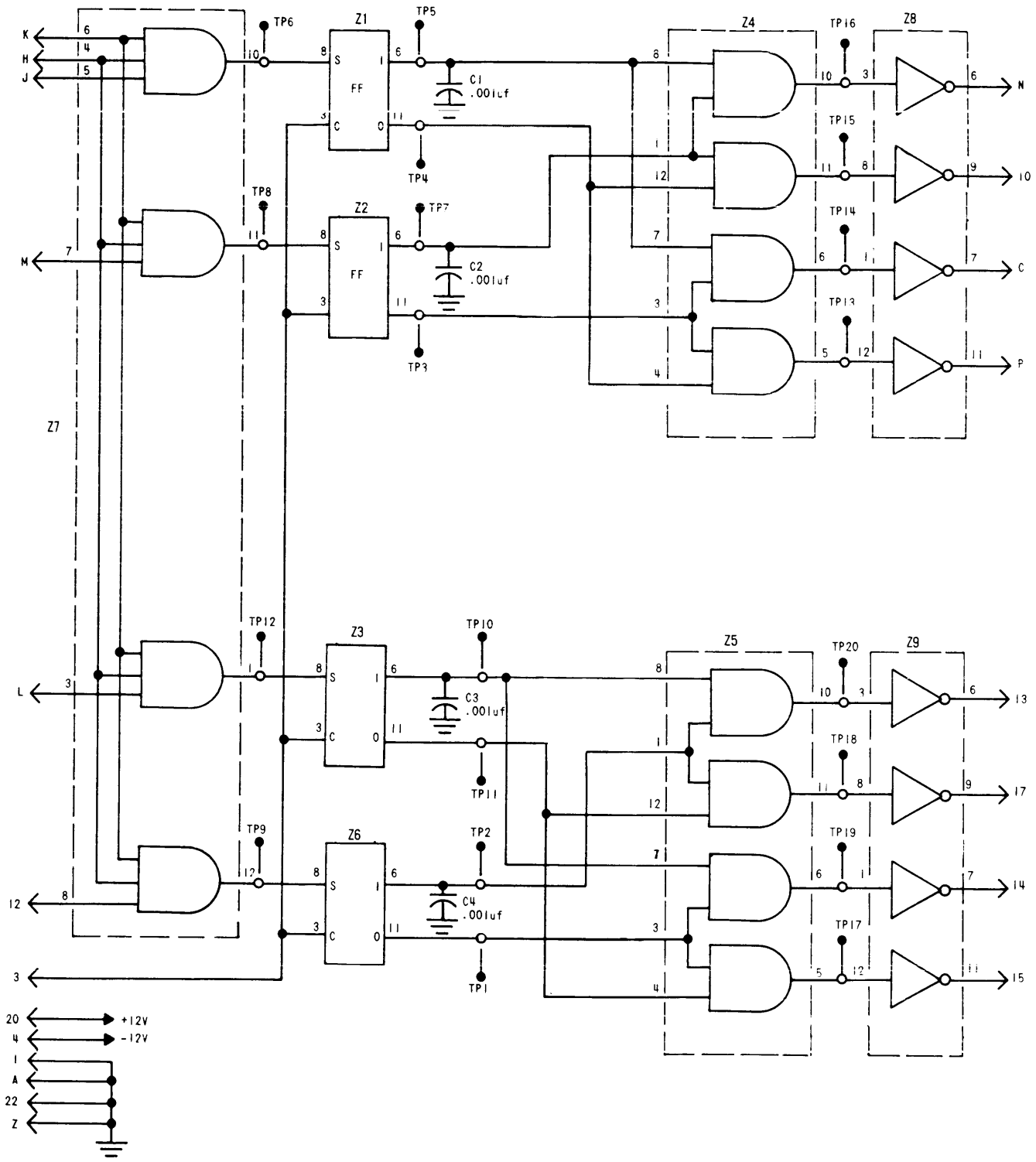


Figure 5-24. Power Supply 2A10, Component Locations



MODULE VOLTAGE & GND CHART			
SYMBOL	PIN CONNECTIONS		
	+12V	-12V	GND
Z1.Z2.Z3.Z6	10	2	5
Z4.Z5.Z7		2	
Z8.Z9	10		5

LAST SYMBOL	MISSING SYMBOL
C4	
TP20	
Z9	

NOTE:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE.

PC396/DA625

Figure 5-25. Memory/Gating Circuits 2A14 and 2A15, Schematic Diagram

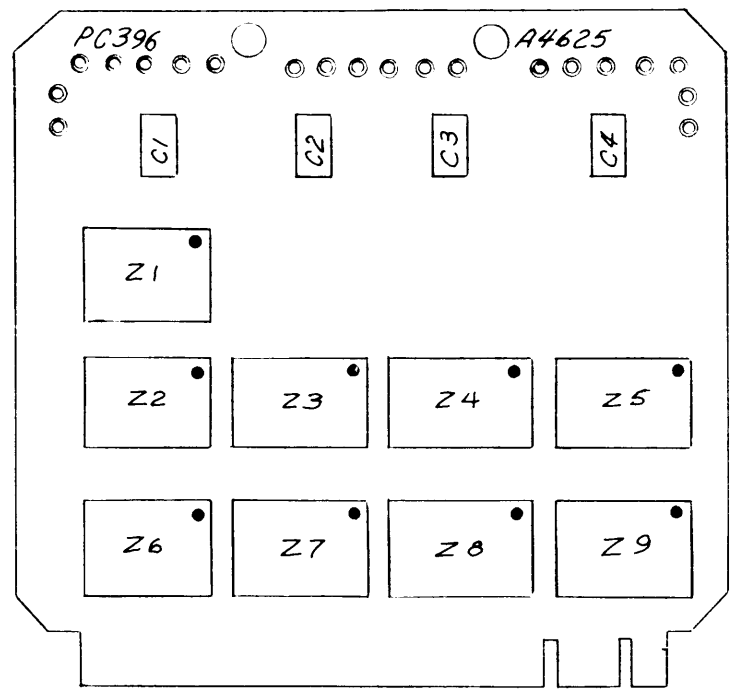
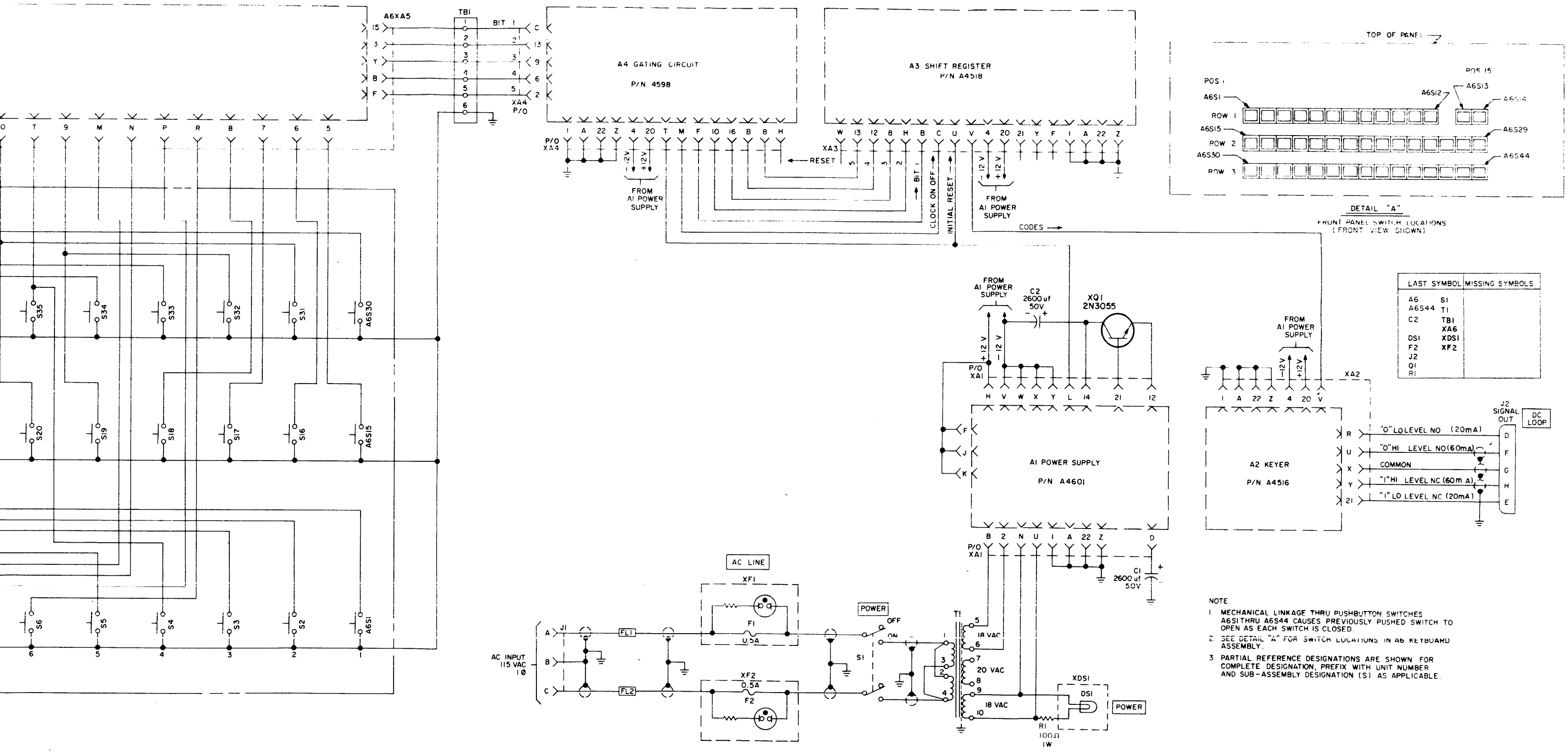


Figure 5-26. Memory/Gating Circuits 2A14 and 2A15, Component Locations



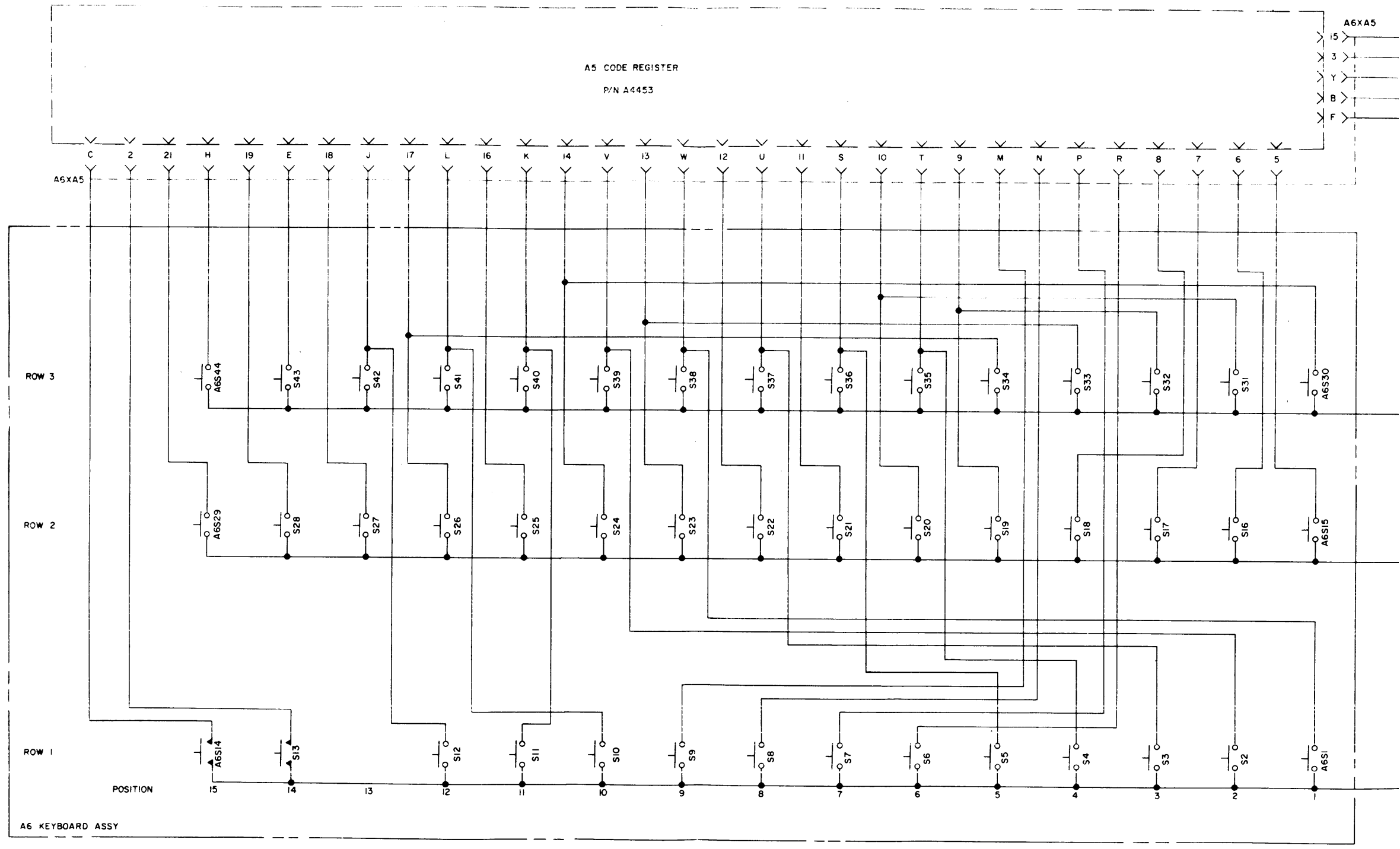
LAST SYMBOL	MISSING SYMBOLS
A6	S1
A6S44	T1
C2	TB1
	XA6
DS1	XDS1
F2	XF2
J2	
Q1	
R1	

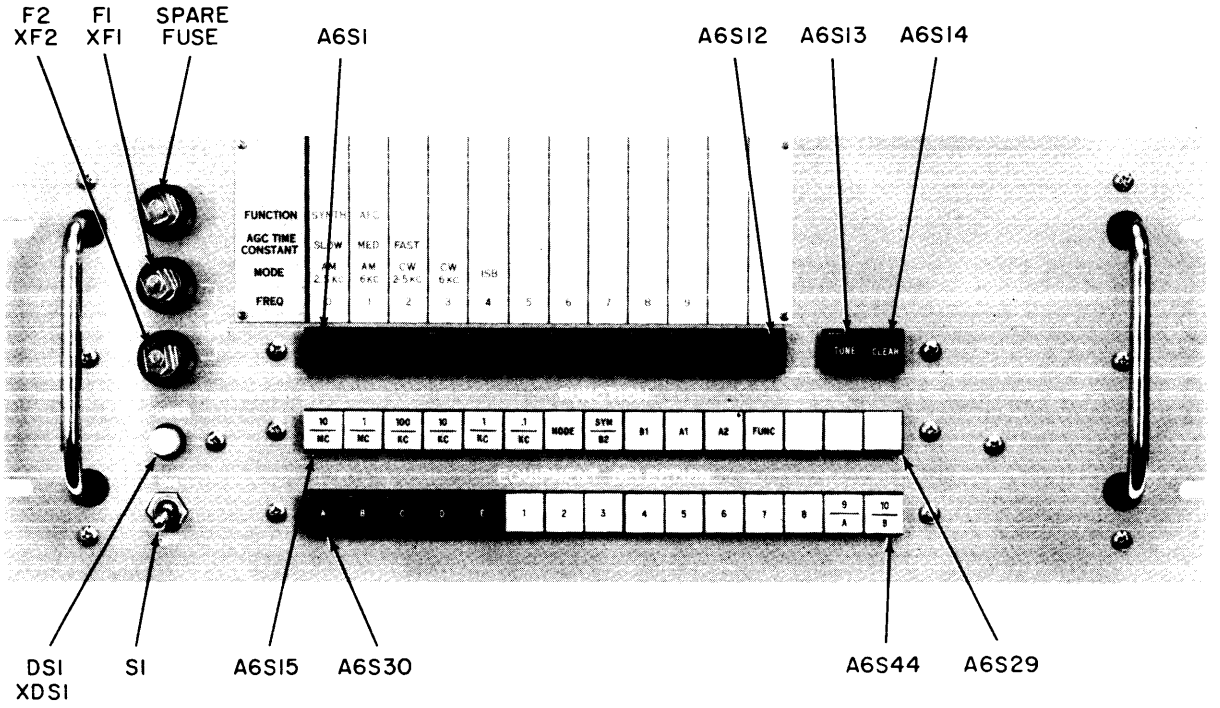
NOTE.

1. MECHANICAL LINKAGE THRU PUSHBUTTON SWITCHES A6S1 THRU A6S44 CAUSES PREVIOUSLY PUSHED SWITCH TO OPEN AS EACH SWITCH IS CLOSED.
2. SEE DETAIL "A" FOR SWITCH LOCATIONS IN A6 KEYBOARD ASSEMBLY.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION (S) AS APPLICABLE.

Figure 5-27. Interconnection Diagram, C-7775/UR

NAVELEX 0967-385-1010





REF DESIG PREFIX 3

Figure 5-28. Major Component Locations, Front Panel of C-7775/UR

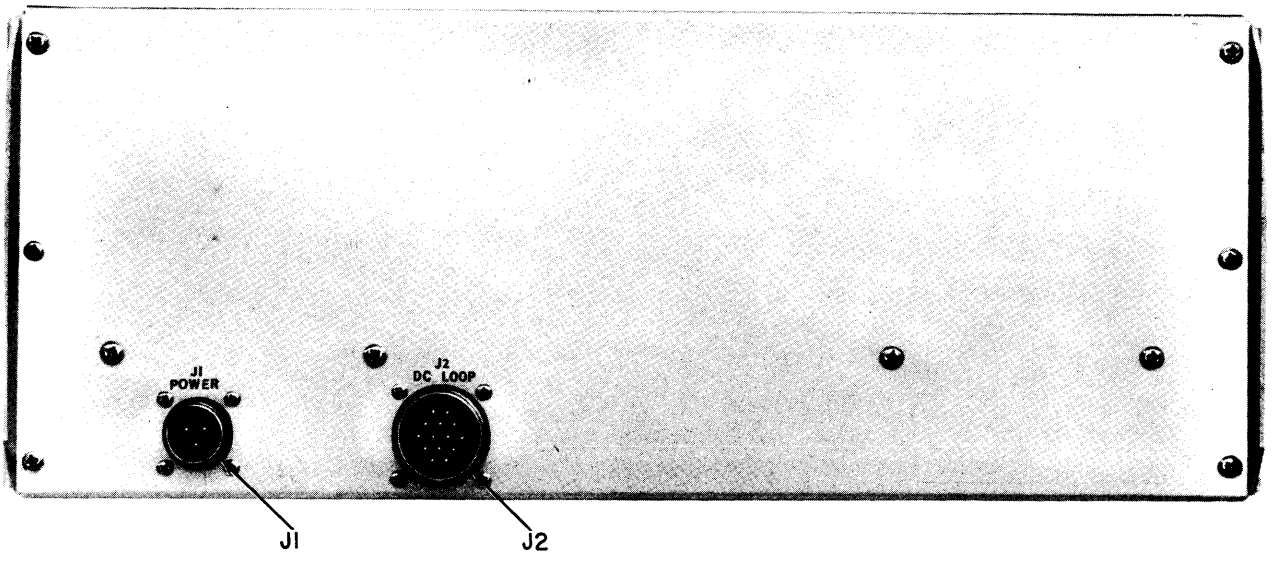


Figure 5-29. Major Component Locations,
Rear Panel of C-7775/UR

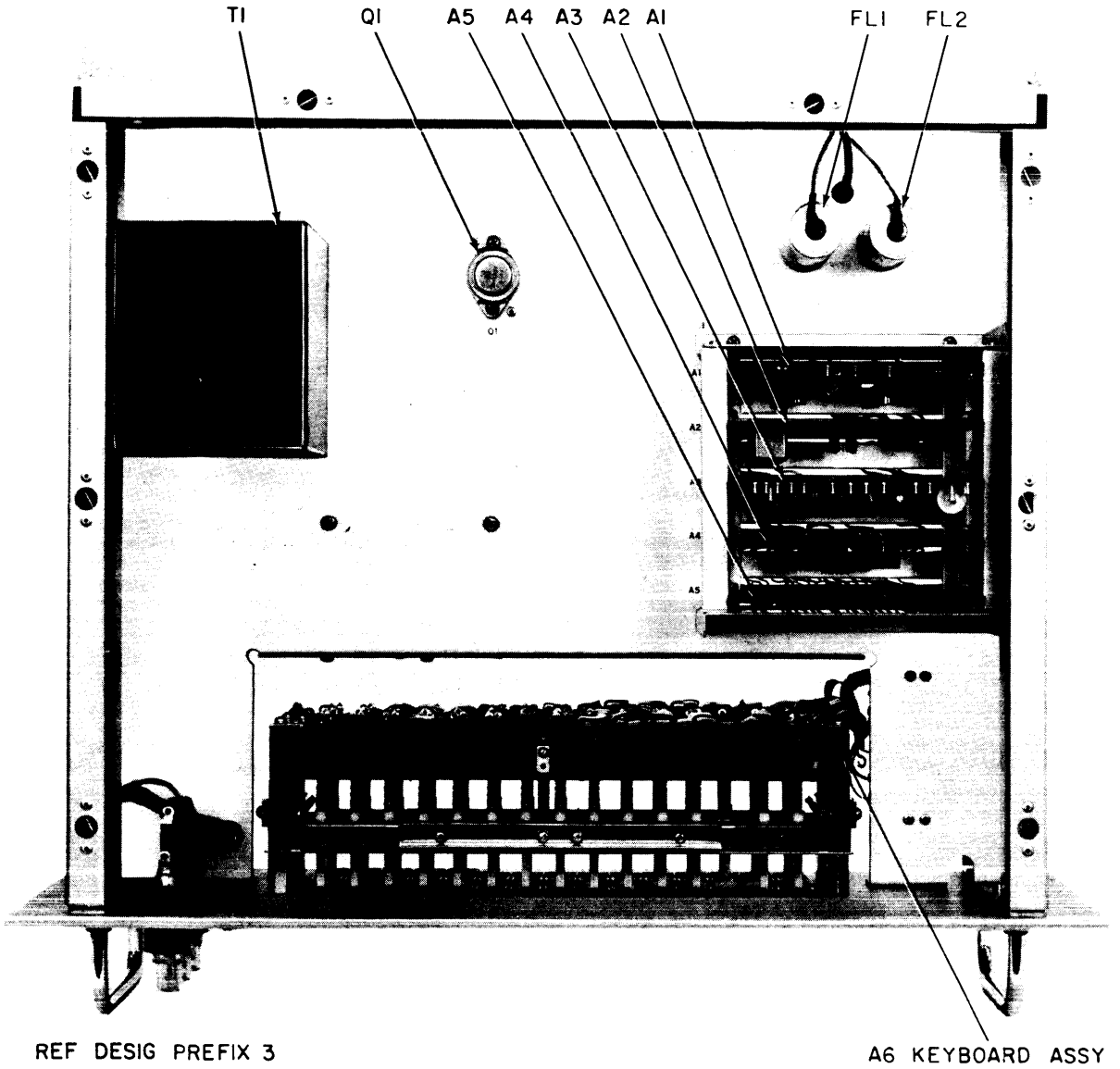


Figure 5-30. Major Component Locations,
Top View of C-7775/UR

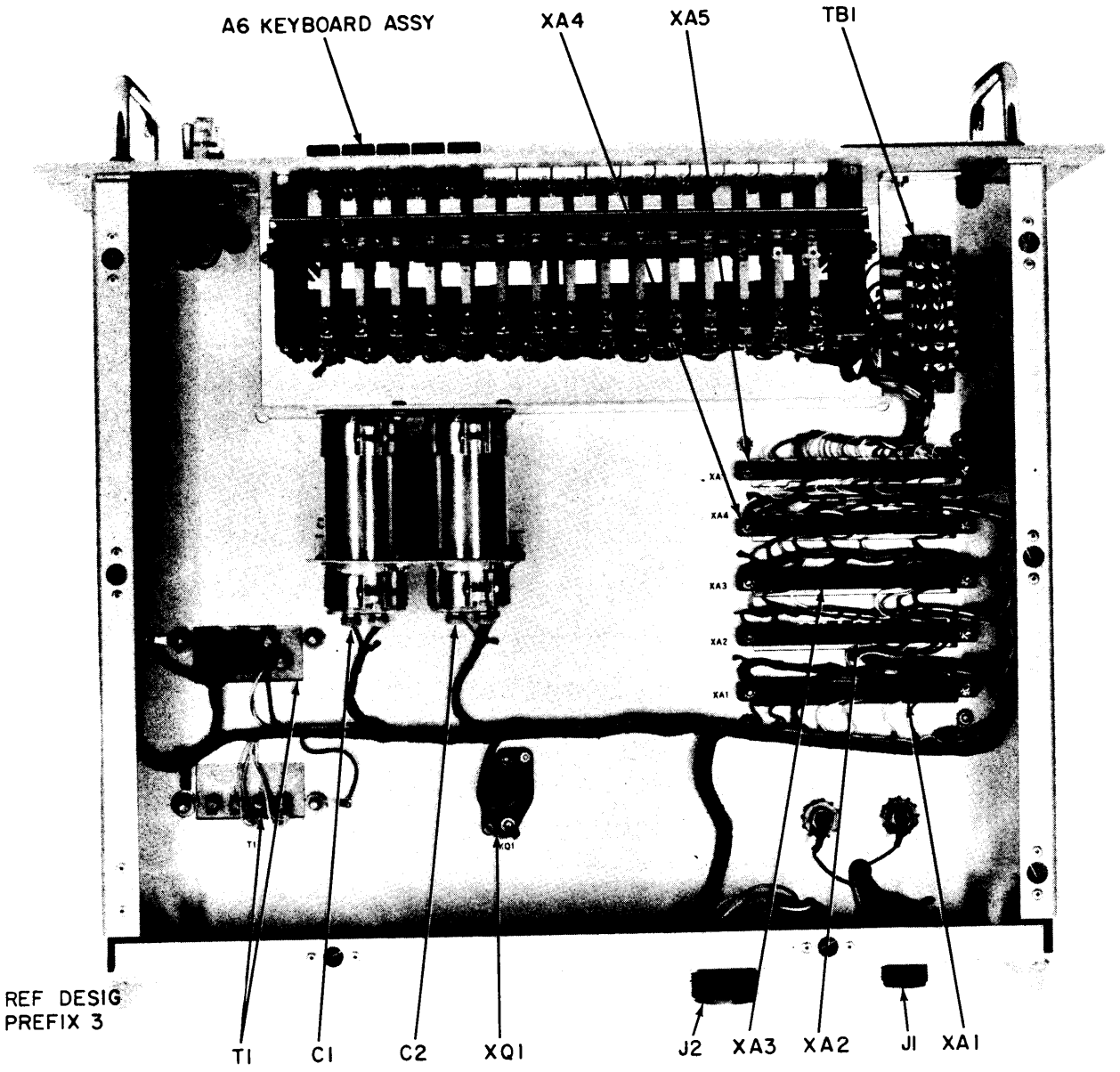
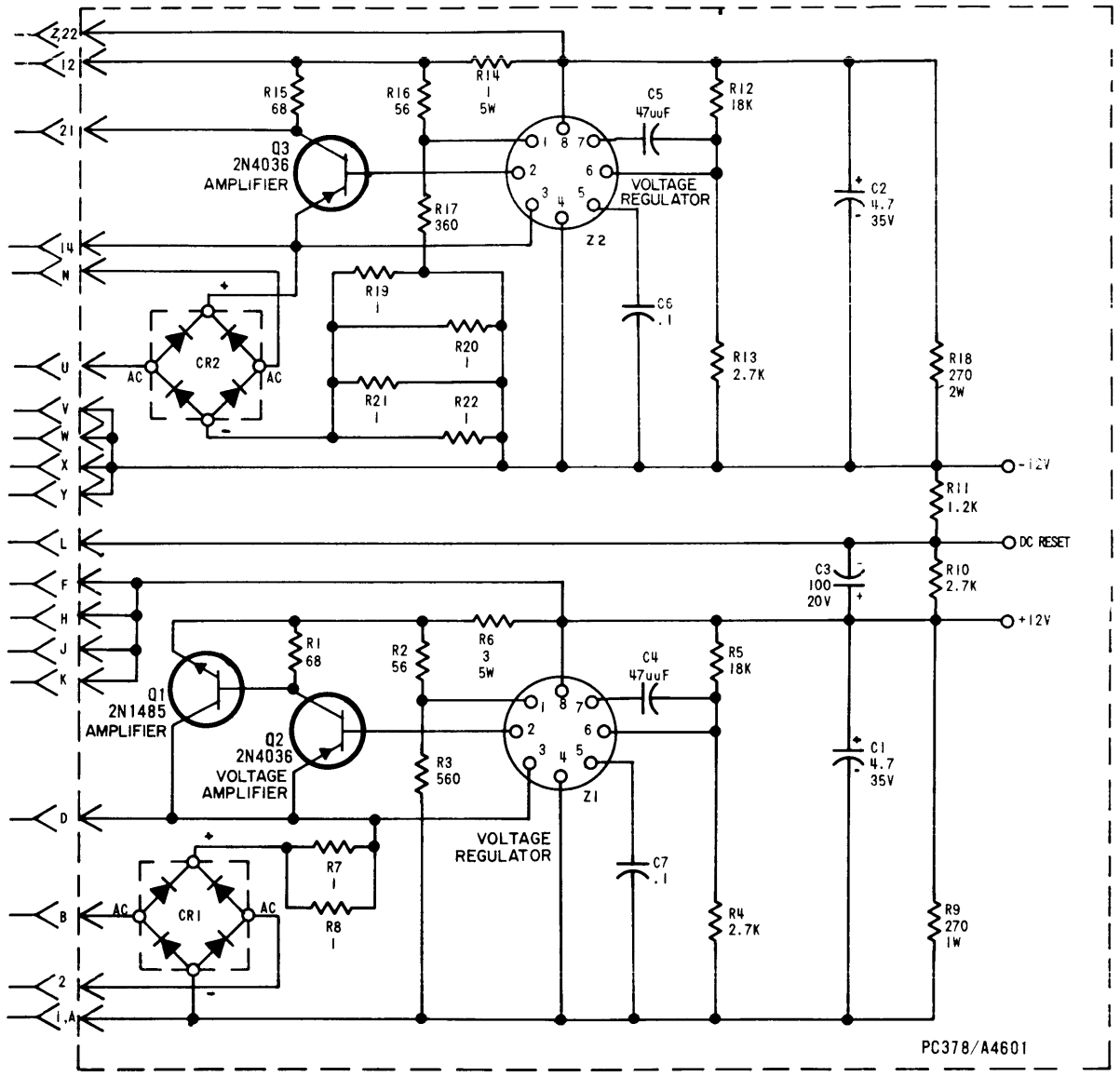


Figure 5-31. Major Component Locations,
Bottom View of C-7775/UR



LAST SYMBOLS	MISSING SYMBOLS
C7	
CR2	
Q3	
R22	
Z2	

UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTANCE VALUES ARE IN OHMS, 1/2W
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE

Figure 5-32. Power Supply 3A1, Schematic Diagram

PART LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC
C1	4D	R7	3F
C2	5D	R8	3F
C3	4E	R9	4F
C4	4F	R10	5E
C5	5F	R11	5D
C6	4G	R12	5E
C7	5G	R13	5E
CR1	3F	R14	5F
CR2	6E	R15	5E
Q1	3D	R16	5E
Q2	3E	R17	5E
Q3	6D	R18	5D
R1	4E	R19	6F
R2	4E	R20	6F
R3	4E	R21	6F
R4	4E	R22	6F
R5	4E	Z1	4F
R6	4F	Z2	5F

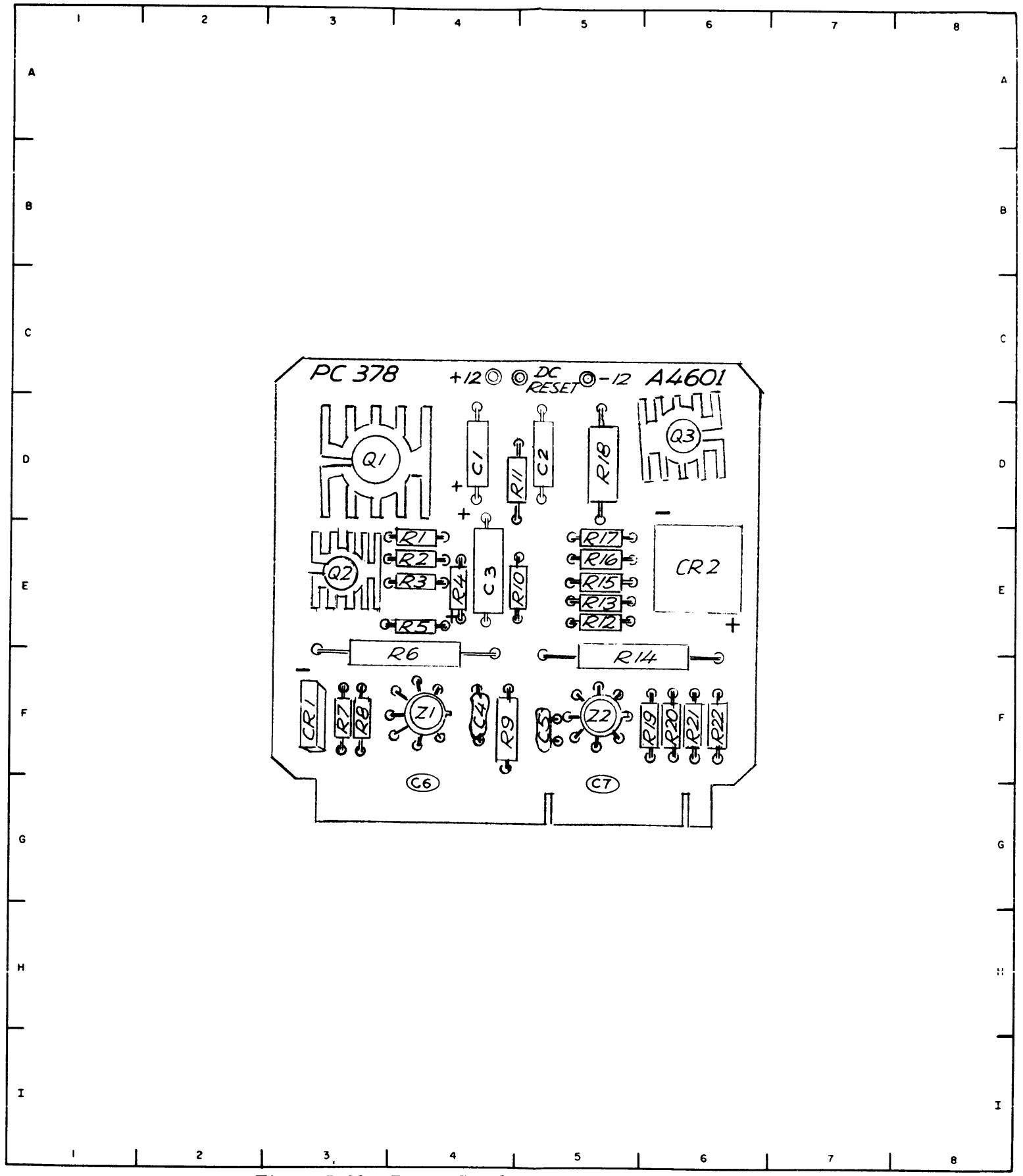
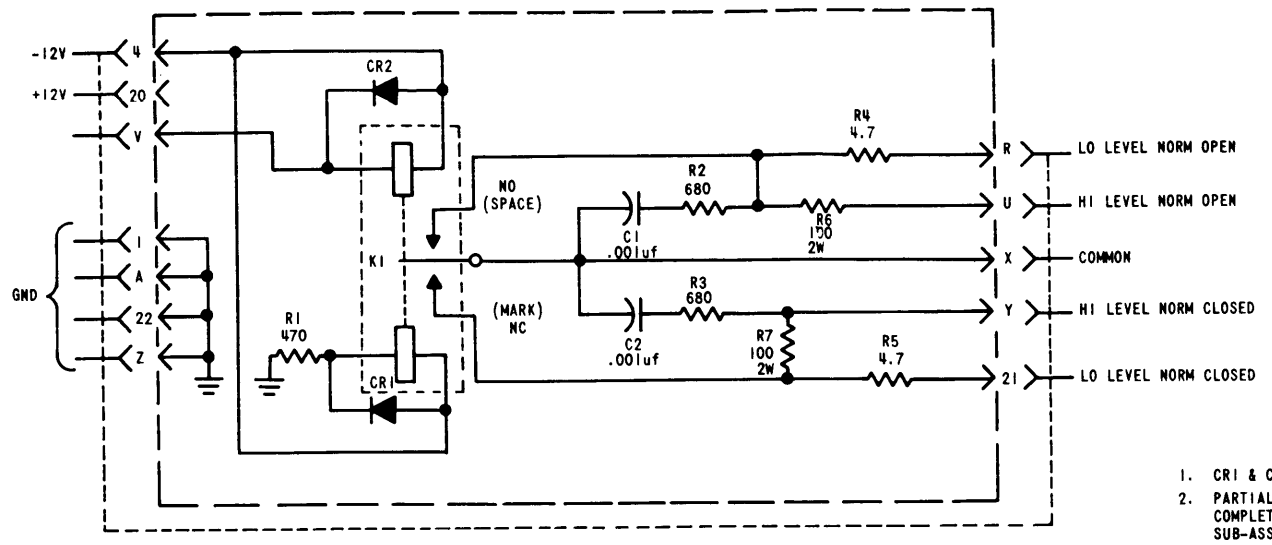


Figure 5-33. Power Supply 3A1, Component Locations



NOTES

1. CR1 & CR2 ARE TYPE 1N4245
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER & SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE

UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/2 WATT

LAST SYMBOLS	MISSING SYMBOLS
C2	
CR2	
K1	
R7	

Figure 5-34. Keyer 3A2, Schematic Diagram

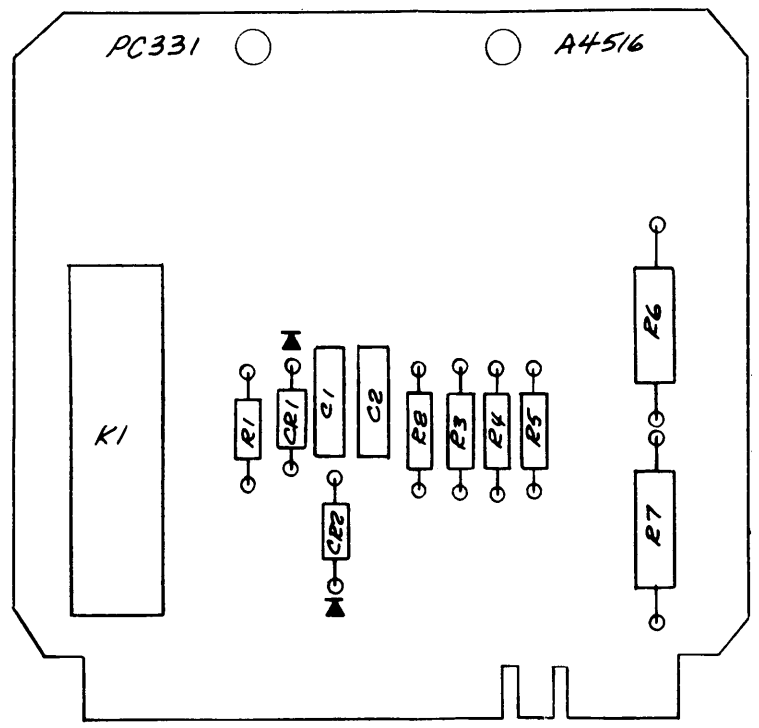
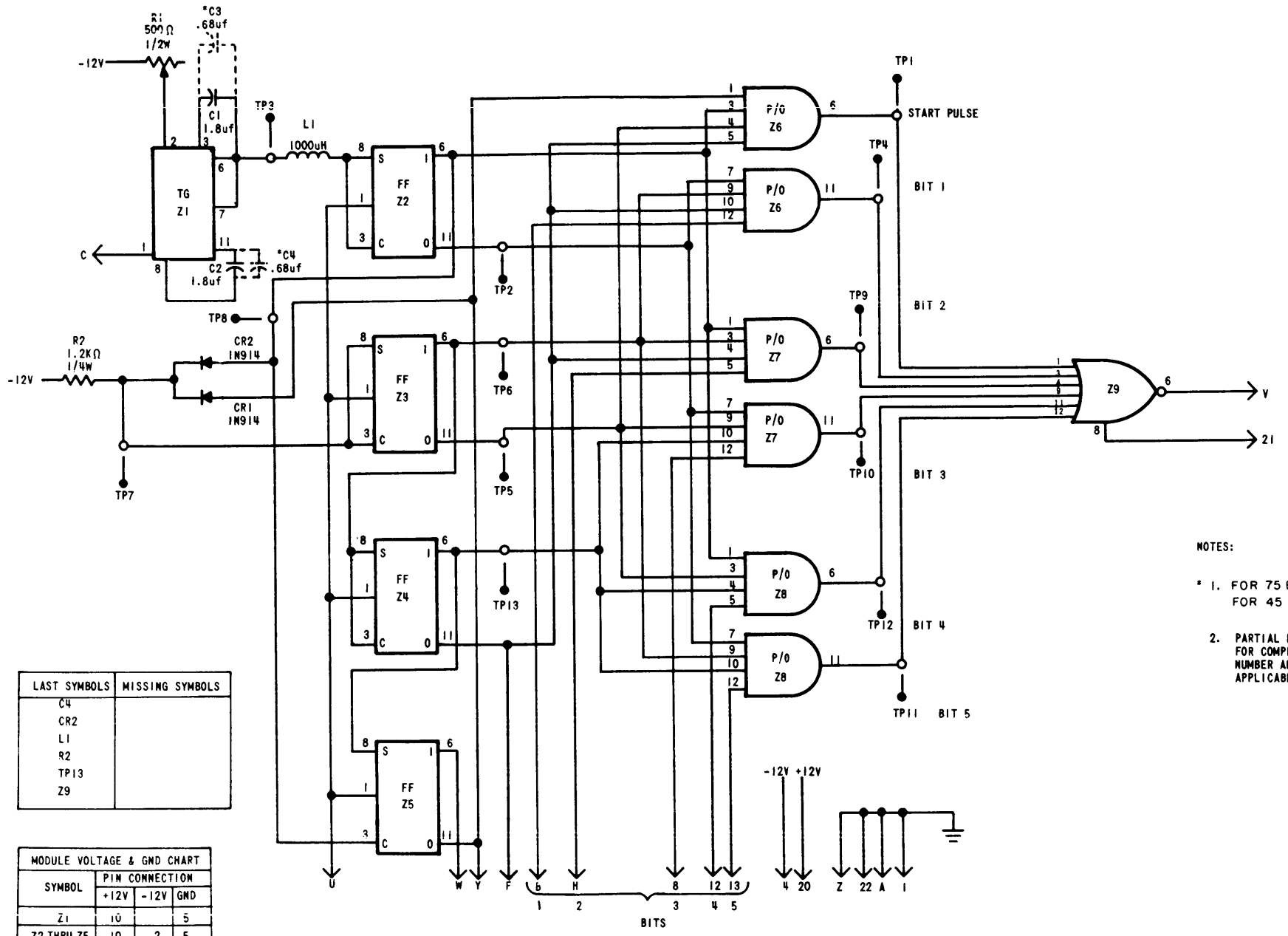


Figure 5-35. Keyer 3A2, Component Locations



LAST SYMBOLS	MISSING SYMBOLS
C4	
CR2	
L1	
R2	
TP13	
Z9	

MODULE VOLTAGE & GND CHART			
SYMBOL	PIN CONNECTION		
	+12V	-12V	GND
Z1	10		5
Z2 THRU Z5	10	2	5
Z6,7,8		2	
Z9	10	2	5

NOTES:

* 1. FOR 75 BAUD OPERATION, DELETE C3 & C4
FOR 45 BAUD OPERATION, ADD C3 & C4

2. PARTIAL REFERENCE DESIGNATION ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE

Figure 5-36. Shift Register 3A3, Schematic Diagram

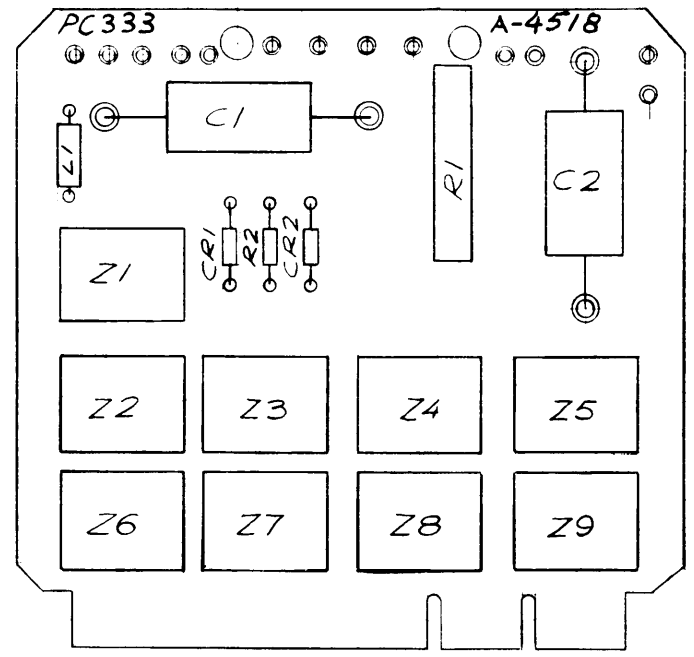
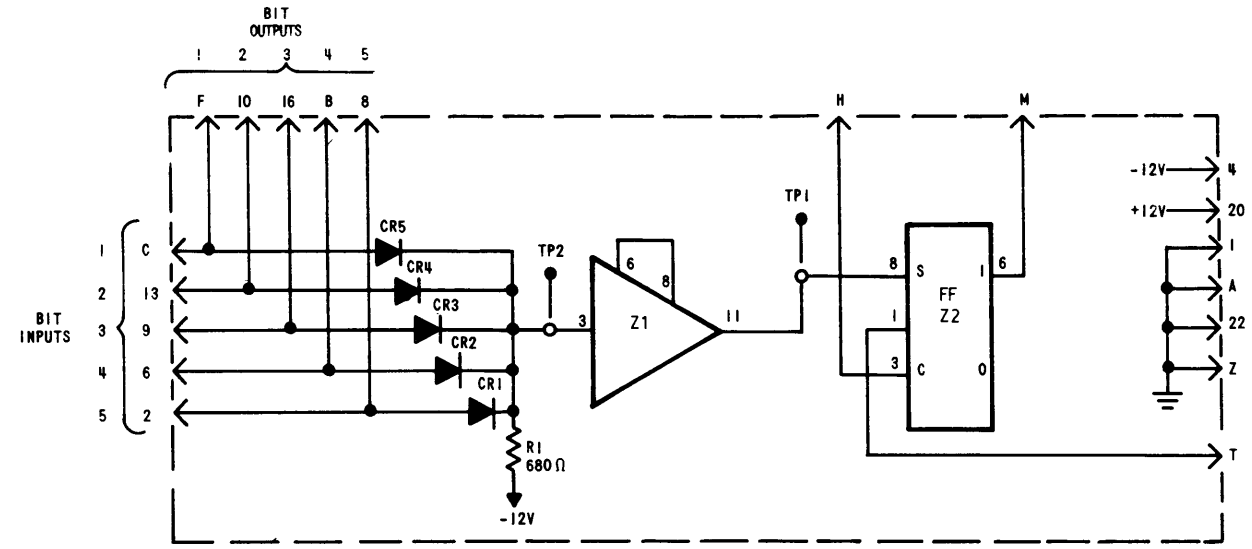


Figure 5-37. Shift Register 3A3,
Component Locations



MODULE VOLTAGE & GND CHART			
	PIN CONNECTION		
SYMBOL	+12V	-12V	GND
Z1	10	2 & 9	4 & 5
Z2	10	2	5

LAST SYMBOL	MISSING SYMBOL
CR5	
R1	
TP2	
Z2	

NOTES:

1- ALL DIODES ARE TYPE 1N914.
2- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION(S) AS APPLICABLE.

Figure 5-38. Gating Circuit 3A4, Schematic Diagram

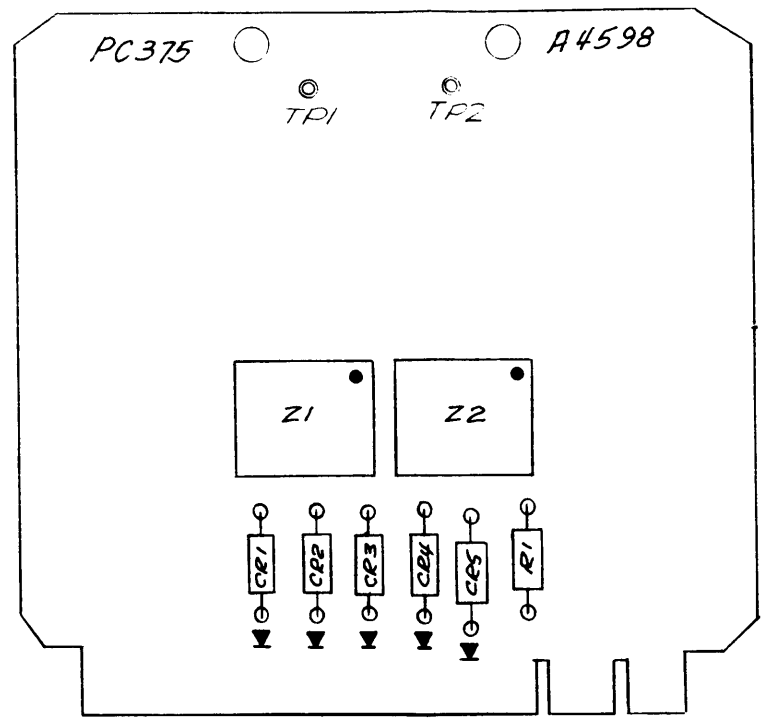
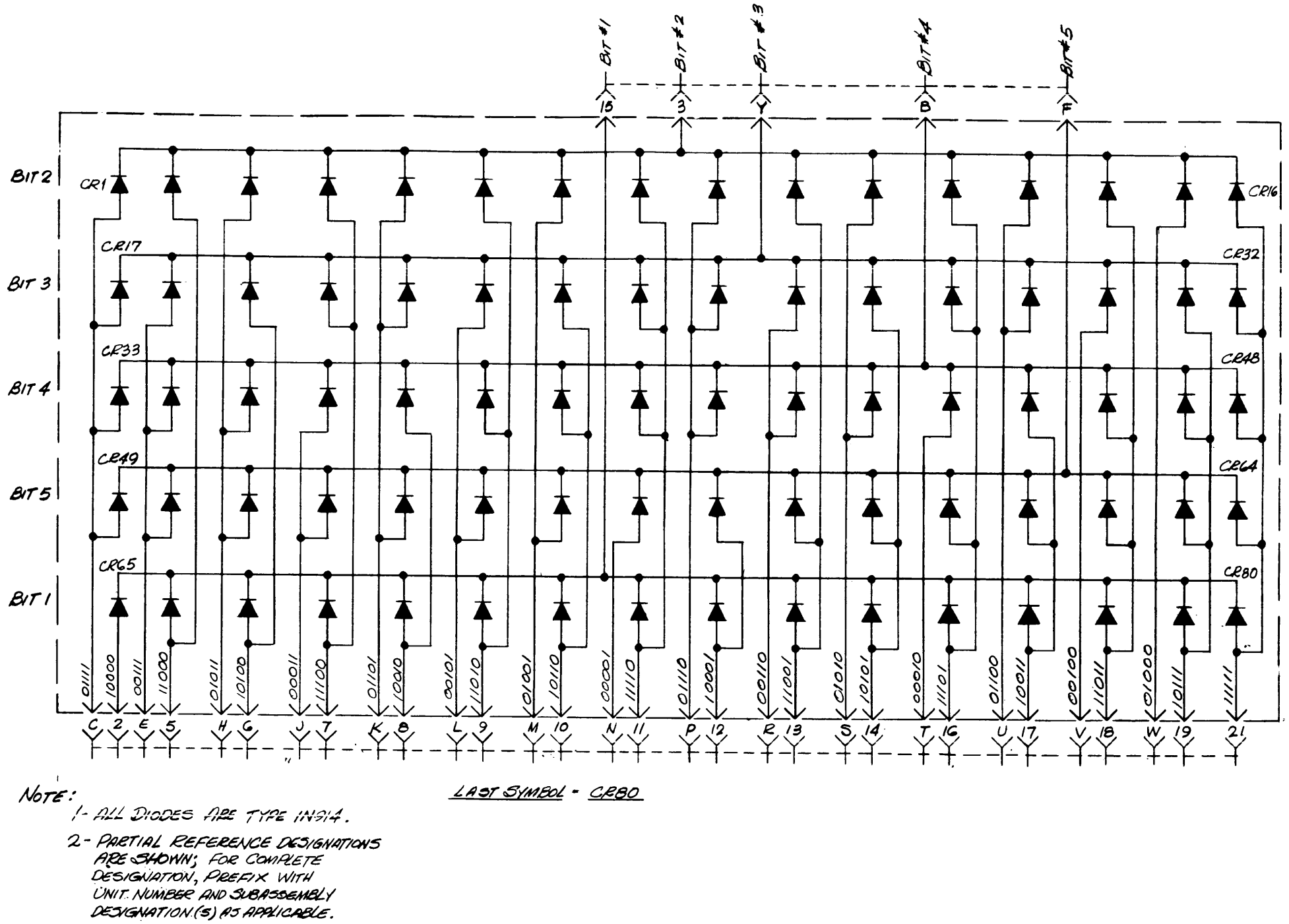


Figure 5-39. Gating Circuit 3A4,
Component Locations



NOTE:
1- ALL DIODES ARE TYPE 1N914.
2- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION(S) AS APPLICABLE.

Figure 5-40. Code Register 3A5, Schematic Diagram

PART LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC
CR1	3D	CR41	5E
CR2	3D	CR42	5E
CR3	3D	CR43	5E
CR4	3D	CR44	5E
CR5	4D	CR45	6E
CR6	4D	CR46	6E
CR7	4D	CR47	6E
CR8	4D	CR48	6E
CR9	5D	CR49	3F
CR10	5D	CR50	3F
CR11	5D	CR51	3F
CR12	5D	CR52	3F
CR13	6D	CR53	4F
CR14	6D	CR54	4F
CR15	6D	CR55	4F
CR16	6D	CR56	4F
CR17	3D	CR57	5F
CR18	3D	CR58	5F
CR19	3D	CR59	5F
CR20	3D	CR60	5F
CR21	4D	CR61	6F
CR22	4D	CR62	6F
CR23	4D	CR63	6F
CR24	4D	CR64	6F
CR25	5D	CR65	3F
CR26	5D	CR66	3F
CR27	5D	CR67	3F
CR28	5D	CR68	3F
CR29	6D	CR69	4F
CR30	6D	CR70	4F
CR31	6D	CR71	4F
CR32	6D	CR72	4F
CR33	3E	CR73	5F
CR34	3E	CR74	5F
CR35	3E	CR75	5F
CR36	3E	CR76	5F
CR37	4E	CR77	6F
CR38	4E	CR78	6F
CR39	4E	CR79	6F
CR40	4E	CR80	6F

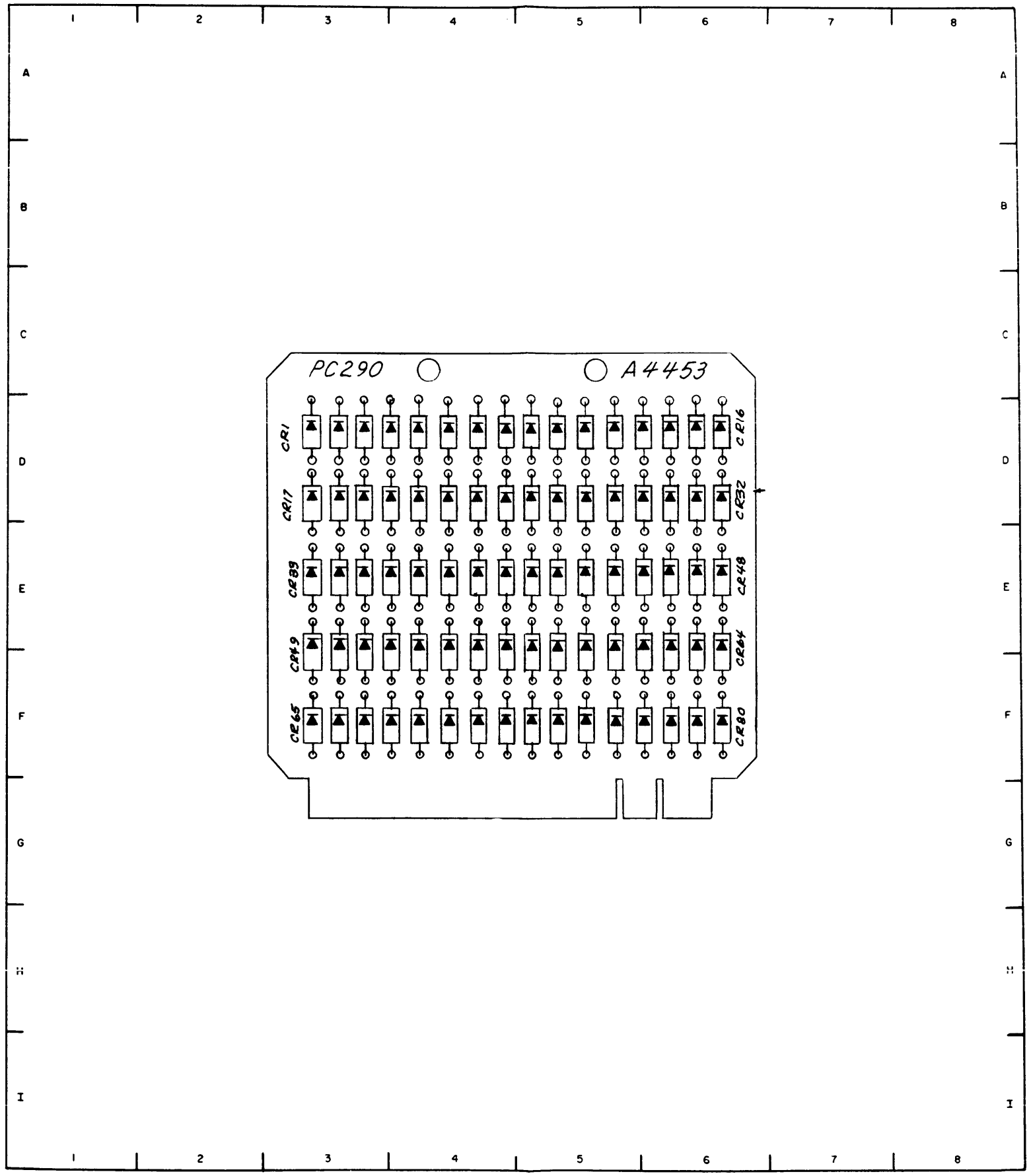


Figure 5-41. Code Register 3A5, Component Locations

NAVELEX 0967-385-1010

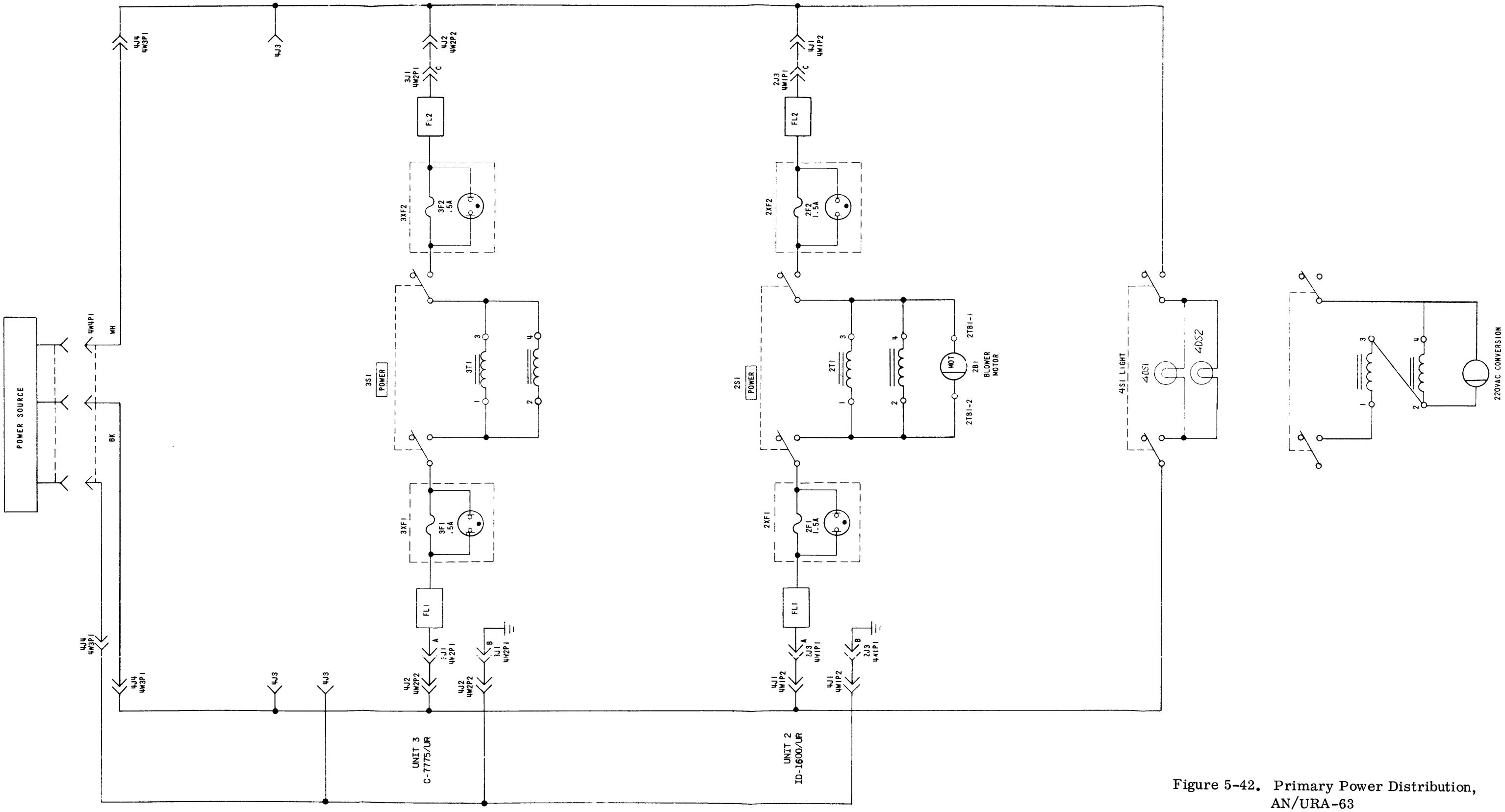
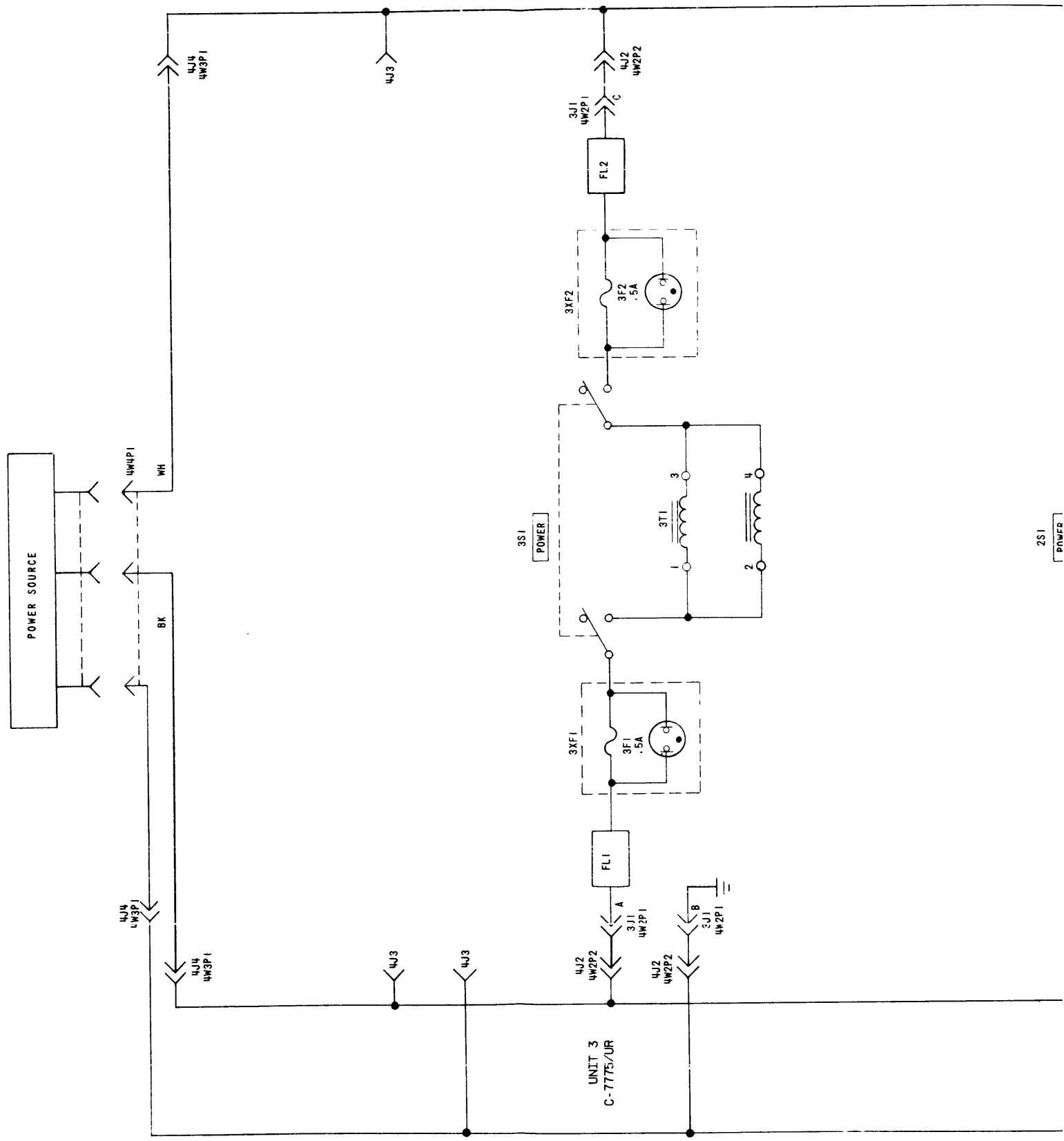


Figure 5-42. Primary Power Distribution, AN/URA-63


4J4
4W3P1
4J3
4J2
4W2P2
3J1
4W2P1
C
FL2
3XF2
3F2
.5A
3S1
POWER
3T1
3
4
1
2
2S1
POWER
4W4P1
WH
BK
POWER SOURCE
3XF1
3F1
.5A
FL1
A
B
3J1
4W2P1
4J4
4W3P1
4J3
4J3
4J2
4W2P2
4J2
4W2P2
UNIT 3
C-7775/UR

ORIGINAL

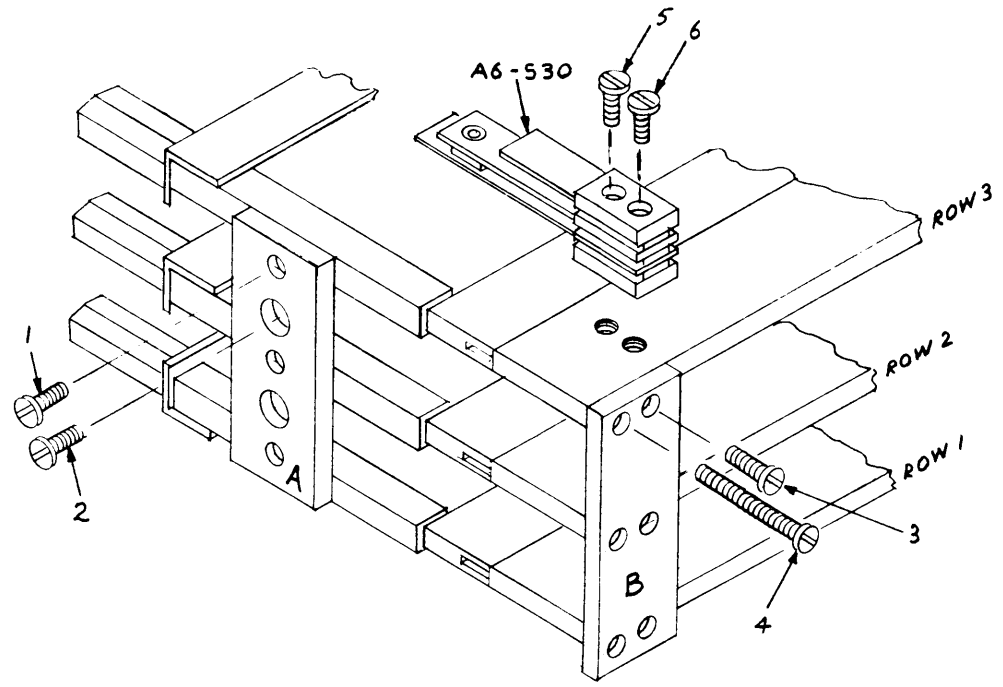


Figure 5-43. Keyboard Assembly 3A6, Exploded View

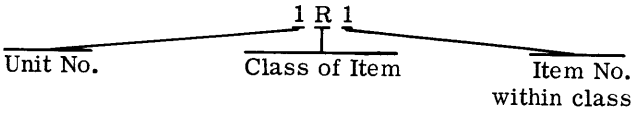
SECTION 6

PARTS LIST

6-1. INTRODUCTION.

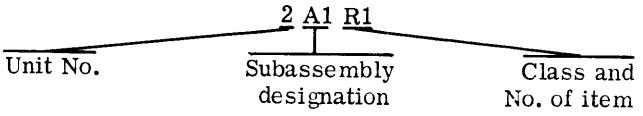
a. REFERENCE DESIGNATIONS. - The unit numbering method of assigning reference designations is used to identify units, assemblies, subassemblies and parts of the AN/URA-63 Communications Control Console. This method is expanded as much as necessary to adequately cover the various degrees of subdivision of the equipment. This unit numbering method and typical expansions of the same are illustrated as follows:

Example 1:



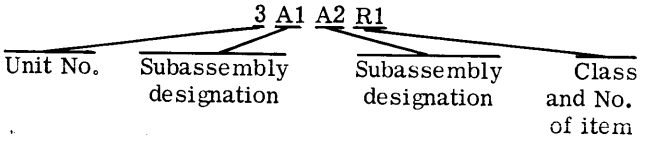
Read as: First (1) resistor (R) of first unit (1).

Example 2:



Read as: First (1) resistor (R) of first (1) subassembly (A) of second (2) unit.

Example 3:



Read as: First (1) resistor (R) of second (2) subassembly (A) of first (1) subassembly (A) of third (3) unit.

b. REFERENCE DESIGNATION PREFIX. - Partial reference designations are used on the equipment and illustrations. The partial reference designations consist of the class letter(s) and the identifying item number. The complete reference designations is obtained by placing the proper prefix before the partial reference designations. Prefixes are provided on illustration following the notation "REF DESIG PREFIX".

6-2. LIST OF UNITS.

Table 6-1 is a listing of the modular units comprising Control Console AN/URA-63. The units are listed by unit numbers in numerical order. Thus when the complete reference designation of a part is known, the table will furnish the identification of the unit in which the part is located, since the first number of a complete reference designation identifies the unit. Table 6-1 also provides the following information for each unit listed: (a) quantity per equipment, (b) official name, (c) designation, (d) colloquial name, and (e) location of the first page of its parts listing in table 6-2.

6-3. MAINTENANCE PARTS LIST.

Table 6-2 is a listing of maintenance parts in each modular unit. The units are listed in numerical sequence. Maintenance parts for each unit are listed in alpha-numerical order by class of part following the unit designation. Thus the parts for each unit are grouped together. Where an identical unit is used more than once, one table serves for all units.

Some small subassemblies are recommended by the manufacturer as non-reparable from a labor or re-alignment cost analysis comparison to the cost of replacing the subassembly. These subassemblies are so noted in the NAME AND DESCRIPTION column and their parts are not included in the list. Other subassemblies are partially reparable, from this point of view. Partially reparable subassemblies are symbollized as "PR" in the NOTES column; their parts are included in the list. Parts that are replaceable are symbollized "R"; parts that are not replaceable are symbollized "NR".

TABLE 6-1. LIST OF UNITS

UNIT	QTY	NAME OF UNIT	DESIGNATION	COLLOQUIAL NAME	PAGE
1	1	Indicator Panel	SB-3230/UR	Indicator Panel, Model RSSA-10	6-2
2	1	Channel/Frequency Indicator	ID-1600/UR	Channel/Frequency Indicator, Model RTIH-3	6-3
3	1	Electronic Command Signal Programmer	C-7775/UR	Programmer, Model RTPH-3	6-10
4	1	Electrical Equipment Cabinet	CY-6538/URA-63	Communications Control Console, Model CON102BJ	6-14

TABLE 6-2. MAINTENANCE PARTS LIST

INDICATOR PANEL, RSSA-10

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
1		RSSA-10, PANEL, INDICATOR: SB 3230/UR Model RSSA-10 is used in conjunction with RTIH-3 to identify specific receivers represented in the RTIH-3.	1-1
1DS1		LAMP, INCANDESCENT: Single contact, T-1-3/4 base, 28 v ac or dc, 0.04 amps, 82679 dwg BI110-10, 08806 P/N 327.	5-3
1DS2 thru 1DS10		SAME AS DS1.	5-3
1J1		CONNECTOR, RECEPTACLE, ELECTRICAL: Provides for 18 male contacts. Phenolic body with rotating screwlock, hood and shell plug. 2.000 in. lg by 0.750 in. wd by 2.125 in. hg. 82679 P/N JJ333-18PR512.	5-3
1XDS1		LIGHT, INDICATOR: White lens cap, engraved black "1", hole mounting socket with solder lug terminals. 0.550 in. dia by 1.279 in. lg. 82679 P/N TS187R1W1B.	5-3
1XDS2		LIGHT, INDICATOR: White lens cap, engraved black "2", hole mounting socket with solder lug terminals. 0.550 in. dia by 1.279 in. lg. 82679 P/N TS107R1W2B.	5-3
1XDS3		LIGHT, INDICATOR: White lens cap, engraved black "3", hole mounting socket with solder lug terminals. 0.550 in. dia by 1.279 in. lg. 82679 P/N TS187R1W3B.	5-3
1XDS4		LIGHT, INDICATOR: White lens cap, engraved black "4", hole mounting socket with solder lug terminals. 0.550 in. dia by 1.279 in. lg. 82679 P/N TS187R1W4B.	5-3
1XDS5		LIGHT, INDICATOR: White lens cap, engraved black "5", hole mounting socket with solder lug terminals. 0.550 in. dia by 1.279 in. lg. 82679 P/N TS187R1W5B.	5-3
1XDS6		LIGHT, INDICATOR: White lens cap, engraved black "6", hole mounting socket with solder lug terminals. 0.550 in. dia by 1.279 in. lg. 82679 P/N TS187R1W6B.	5-3
1XDS7		LIGHT, INDICATOR: White lens cap, engraved black "7", hole mounting socket with solder lug terminals. 0.550 in. dia by 1.279 in. lg. 82679 P/N TS187R1W7B.	5-3
1XDS8		LIGHT, INDICATOR: White lens cap, engraved black "8", hole mounting socket with solder lug terminals. 0.550 in. dia by 1.279 in. lg. 82679 P/N TS187R1W8B.	5-3
1XDS9		LIGHT, INDICATOR: White lens cap, engraved black "9", hole mounting socket with solder lug terminals. 0.550 in. dia by 1.279 in. lg. 82679 P/N TS187R1W9B.	5-3
1XDS10		LIGHT, INDICATOR: White lens cap, engraved black "10", hole mounting socket with solder lug terminals. 0.550 in. dia by 1.279 in. lg. 82679 P/N TS187R1W10B.	5-3

TABLE 6-2. MAINTENANCE PARTS LIST (Continued)

CHANNEL/FREQUENCY INDICATOR, RTIH-3

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
2		RTIH-3, INDICATOR, CHANNEL/FREQUENCY: ID-1600/UR. Monitor unit for remote tuning system which has control positions.	1-1
2A1		CIRCUIT CARD ASSEMBLY: 4 capacitors, 11 integrated circuits, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4492.	5-7
2A2		CIRCUIT CARD ASSEMBLY: 6 resistors, 3 capacitors, 1 relay, 1 transistor, 4 semiconductors, plug-in type; 4.375 in. lg by 4.125 in. wd by 0.375 in. hg. 82679 P/N A4494.	5-7
2A3		CIRCUIT CARD ASSEMBLY: 1 resistor, 1 capacitor, 14 integrated circuits, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4531.	5-7
2A4		CIRCUIT CARD ASSEMBLY: 15 integrated circuits, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4495.	5-7
2A5		SAME AS 2A4.	5-7
2A6		CIRCUIT CARD ASSEMBLY: 12 integrated circuits, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4493.	5-7
2A7		SAME AS 2A6.	5-7
2A8		CIRCUIT CARD ASSEMBLY: 2 capacitors, 1 resistor, 14 integrated circuits, 4 semiconductors, plug-in type; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4530.	5-7
2A9		CIRCUIT CARD ASSEMBLY: 5 resistors, 3 capacitors, 10 integrated circuits, 4 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4496.	5-7
2A10		CIRCUIT CARD ASSEMBLY: 17 resistors, 4 capacitors, 2 integrated circuits, 4 transistors, 2 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4545.	5-7
2A11		NOT USED.	5-7
2A12		NOT USED.	5-7
2A13		NOT USED.	5-7
2A14		CIRCUIT CARD ASSEMBLY; 4 capacitors, 9 integrated circuits, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4625.	5-7
2A15		SAME AS 2A14.	5-7
2A16		SAME AS 2A1.	5-7
2B1		FAN, AXIAL: 115 vac, 50/60 cps, CMF-45 at 60 cps, free delivery. Plastic blade, aluminum housing with black enamel finish. 3.625 in. by 3.625 in. by 1.500 in. o/a. 82679 P/N BL131.	5-7
2C1		CAPACITOR, FIXED, ELECTROLYTIC: 1200 uf, 40 vdcw, 2.063 in. dia by 4.500 in. lg. dwg CE112-12, 80183 P/N 36D123G040BC2A.	5-8
2C2		CAPACITOR, FIXED, ELECTROLYTIC: 2600 uf, 50 vdcw, 1.438 in. dia by 3.500 in. lg. dwg CE112-6, 80183 P/N 36D262G050AB6B.	5-8
2C3		CAPACITOR, FIXED, ELECTROLYTIC: 100 uf, 450 vdcw, 1.438 in. dia by 3.500 in. lg. dwg CE112-13, 80183 P/N 36D101G450AB6A.	5-8
2CR1		RECTIFIER, SEMICONDUCTOR DEVICE: 100 PIV per leg dc or recurrent volts; full wave rectification. 1.125 in. lg by 1.125 in. wd by 0.406 in. hg. 82679 P/N RX108-2.	5-8
2CR2		SEMICONDUCTOR DEVICE, DIODE: MIL type 1N3015B.	5-7
2DS1		LAMP, INCANDESCENT: Single contact, T-1-3/4 base, 28 v ac or dc, 0.04 amps. dwg BI110-10, 08806 P/N 330.	5-5

TABLE 6-2. MAINTENANCE PARTS LIST (Continued)

CHANNEL/FREQUENCY INDICATOR, RTIH-3

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
2DS2 thru 2DS9		SAME AS 2DS1.	5-5
2DS10		INDICATOR, DIGITAL DISPLAY: Displays numerals 0 thru 9, minimum supply voltage 170 vdc, 14 pin type terminals, 1.020 in. dia by 1.120 in. hg from mtg surface. 82679 P/N BI118.	5-5
2DS11		SAME AS 2DS10.	5-5
2DS12		LAMP, GLOW: 110-125 vac, cylindrical clear lens. 0.284 in. dia by 1.328 in. lg. dwg BI119-HL7. 72619 P/N 507-3836-1531-600.	5-5
2DS13 thru 2DS16		SAME AS 2DS10.	5-5
2DS17 thru 2DS19		NOT USED.	5-5
2DS20		INDICATOR, DIGITAL READOUT: Socket and lamp assembly. Six 14 volt lamps. 3.467 in. lg by 0.745 in. wd by 1.110 in. hg. dwg IC105-1, 05464 P/N 13377-01-7155-022.	5-5
2DS21		SAME AS 2DS22.	5-5
2DS22		INDICATOR, DIGITAL READOUT: Socket and lamp assembly. Six 14 volt lamps. 3.467 in. lg by 0.745 in. wd by 1.110 in. hg. dwg IC105-2, 05464 P/N 13377-01-6027-022.	5-5
2F1		FUSE, CARTRIDGE TYPE: 0.5 amp, 125 v 0.250 in. dia by 1.250 in. lg. dwg FU102-3, 71400 P/N MDL-3.	5-5
2F2		SAME AS 2F1.	5-5
2FL1		FILTER, RADIO INTEREFERENCE: 5 amp current, 600 vdc, 250 vac at 60 cps. 1.000 in. dia by 2.688 in. lg dwg FI105-2, 80183 P/N 5JX100.	5-8
2FL2		SAME AS FL1.	5-6
2J1		CONNECTOR: MIL type MS3102A20-29S.	5-6
2J2		CONNECTOR: MIL type MS3102A20-27P.	5-6
2J3		CONNECTOR: MIL type MS3102A14S1P.	5-7
2Q1		TRANSISTOR: MIL type 2N3055.	5-7
2R1		RESISTOR: MIL type RE75GR2501.	5-7
2R2		RESISTOR: MIL type RE65GR250.	5-8
2R3		SAME AS 2R2.	5-8
2S1		SWITCH: MIL type ST22K.	5-5
2T1		TRANSFORMER, POWER, STEP-UP, STEP DOWN: Primary; 115/230V, 50/60 cps, 1 phase: secondary; 20 v, 6A dc, 20 v, 600 madc, 280 v CT, 25 madc, 15 v, 65 MADC. Hermetically sealed metal case; stud mounted. 13 solder stud terminals. 5.000 in. lg by 4.375 in. wd by 3.750 in. hg. 82679 P/N TF355.	5-8
2TB1		TERMINAL BOARD: Barrier type; two 6-32 thd single screw lugs. Phenolic body 0.406 in. by 0.875 in. by 1.500 in. dwg TM100-2, 86178 P/N 2-164YD.	5-7
2XA1		CONNECTOR, RECEPTACLE, ELECTRICAL: 22 double sided female contacts rated at 5 amps and 1,800 v rms. Phenolic housing with floating bushing and eyelet terminals. Accepts printed circuit board thickness of 0.054 in. to 0.071 in. 82679 P/N JJ319-22-DFE.	5-7
2XA2 thru 2XA19		SAME AS 2XA1.	5-7
2XDS1 thru 2XDS4		LIGHT INDICATOR: Green lens. 1.35 to 28 v T-1-3/4 lamp base. 2 terminals. 0.437 in. dia by 1.500 in. lg, dwg TS153-9, 72619 P/N 162-8430-1472-502.	5-5
2XDS5		LIGHT, INDICATOR: Yellow lens, 1.35 to 28 v T-1-3/4 lamp base, 2 terminals. 0.437 in. dia by 1.500 in. lg. dwg TS153-10, 72619 P/N 162-8430-1473-502.	5-5

TABLE 6-2. MAINTENANCE PARTS LIST (Continued)

CHANNEL/FREQUENCY INDICATOR, RTIH-3

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
2XDS6		SAME AS 2XDS5.	5-5
2XDS7		LIGHT, INDICATOR: Red lens. 1.35 to 28 v T-1-3/4 lamp base. 2 terminals. 0.437 in. dia by 1.500 in. lg. dwg TS153-8, 72619 P/N 162-8430-1471-502.	5-5
2XDS8		SAME AS 2XDS7.	5-5
2XDS9		SAME AS 2XDS7.	5-5
2XDS10		SOCKET, ELECTRON TUBE: 14 silver plated beryllium copper contacts. 1.562 in. lg by 0.750 in. wd by 0.646 in. hg. dwg TS192, 83594 P/N SK136.	5-5
2XDS11		SAME AS 2XDS10.	5-5
2XDS12		SOCKET, LAMP: 110-125 vac, 0.375 in. dia by 1.000 in. lg. dwg TS193-1, 72619 P/N 515-0012.	5-5
2XDS13 thru 2XDS16		SAME AS 2XDS10.	5-5
2XDS17		CONNECTOR, RECEPTACLE, ELECTRICAL: 14 contacts, 2 rows of 7 each. 0.250 in. wd by 1.500 in. lg by 0.410 in. hg. 82679 P/N JJ350.	5-5
2XDS18 thru 2XDS25		SAME AS 2XDS17.	5-5
2XF1		FUSEHOLDER, LAMP INDICATING: 15 amps, neon lamp, clear knob, accommodates 1/4 in. dia by 1.250 in. lg fuse. dwg FH104-3, 71400 P/N HKL-X.	5-5
2XF2		SAME AS 2XF1.	5-5
2ZX1 thru 2ZX9		NOT USED.	
2ZX10		INTEGRATED CIRCUIT, DECODER: 200 ±10 vdc at 4.0 ma. Provides circuitry for indicator, digital display. 12 pins. 0.989 in. dia by 1.641 in. lg. 82679 P/N IC104.	5-7
2ZX11 thru 2ZX16		SAME AS 2ZX10.	5-7
2A1		CIRCUIT CARD ASSEMBLY: 4 capacitors, 11 integrated circuits, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4492.	5-10
2A1C1		CAPACITOR, FIXED, CERAMIC: 1,000 uuf, GMV, 500 vdcw, 0.310 in. dia by 0.156 in. thk, 0.250 in. lead spacing. 82679 P/N CC100-29.	5-10
2A1C2 thru 2A1C4		SAME AS 2A1C1.	5-10
2A1Z1		INTEGRATED CIRCUIT, DIGITAL FLIP FLOP: 11 pins, plastic case; supply voltage -9.5 v 0.895 in. lg by 0.678 in. wd by 0.495 in. hg. 82679 P/N NW151.	5-10
2A1Z2		SAME AS 2A1Z1.	5-10
2A1Z3		SAME AS 2A1Z1.	5-10
2A1Z4		SAME AS 2A1Z1.	5-10
2A1Z5		INTEGRATED CIRCUIT, DIGITAL AND GATE: 11 pins, plastic case; supply voltage, -12 v, 0.875 in. lg by 0.625 in. wd by 0.438 in. hg. 82679 P/N NW142-44.	5-10
2A1Z6		INTEGRATED CIRCUIT, DIGITAL INVERTER: 11 pins, plastic case; supply voltage variable by usage. 0.875 in. lg by 0.625 in. wd by 0.938 in. hg. 82679 P/N NW150-4.	5-10
2A1Z7		SAME AS 2A1Z5.	5-10
2A1Z8		SAME AS 2A1Z6.	5-10

TABLE 6-2. MAINTENANCE PARTS LIST (Continued)

CHANNEL/FREQUENCY INDICATOR, RTIH-3

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
2A1Z9		INTEGRATED CIRCUIT, DIGITAL AND GATE: 11 pins, plastic case, 12 v logic. 0.865 in. lg. by 0.678 in. wd by 0.495 in. hg. 82679 P/N NW142-31.	5-10
2A1Z10		SAME AS 2A1Z6.	5-10
2A1Z11		SAME AS 2A1Z5.	5-10
2A2		CIRCUIT CARD ASSEMBLY: 6 resistors, 3 capacitors, 1 relay, 1 transistor, 4 semiconductors, plug-in type; 4.375 in. lg by 4.125 in. wd by 0.375 in. hg. 82679 P/N A4494.	5-12
2A2C1		CAPACITOR, FIXED, MICA: 1,000 uuf, ±1/2% tol, 100 vdcw. 0.640 in. lg by 0.591 in. wd by 0.198 in. thk, 82679 P/N CM11F102D1S.	5-12
2A2C2		CAPACITOR: MIL type CL65BG101KP3.	5-12
2A2C3		SAME AS 2A2C2.	5-12
2A2CR1		SEMICONDUCTOR DEVICE: MIL type 1N4245.	5-12
2A2CR2		SAME AS 2A2CR1.	5-12
2A2CR3		SAME AS 2A2CR1.	5-12
2A2CR4		RECTIFIER, SEMICONDUCTOR DEVICE: 1.5 vdc output current, 200 peak reverse v. 0.688 in. wd by 0.469 in. hg by 0.250 in. thk. 82679 P/N DD130-200-1.5.	5-12
2A2K1		RELAY, ARMATURE: Mercury wetted contacts rated at 2 amps mac, 500 v max. 2 windings rated at 250 ohms each ±10%. 2.063 in. lg by 0.625 in. hg by 0.625 in. wd. wire lead mounted. 82679 P/N RL167-1.	5-12
2A2Q1		TRANSISTOR: MIL type 2N3013.	5-12
2A2R1		RESISTOR: MIL type RC20GF472J.	5-12
2A2R2		RESISTOR: MIL type RC20GF271J.	5-12
2A2R3		SAME AS 2A2R1.	5-12
2A2R4		RESISTOR, VARIABLE, COMPOSITION: 1,000 ohms, ±10% tol, clockwise modified log tape. 0.500 in. lead mounted. 82679 P/N RV111-U-102A.	5-12
2A2R5		RESISTOR: MIL type RC32GF101J.	5-12
2A2R6		RESISTOR: MIL type RC32GF221J.	5-12
2A3		CIRCUIT CARD ASSEMBLY: 1 resistor, 1 capacitor, 14 integrated circuits; plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4531.	5-14
2A3C1		CAPACITOR, FIXED, ELECTROLYTIC: 20 uf, -10% +150% at 125 cps, 25°C, 25 vdcw. 0.312 in. dia by 0.750 in. lg. dwg CE105-20-25, 14655 P/N NLW20-25.	5-14
2A3R1		RESISTOR: MIL type RC07GF182J.	5-14
2A3Z1 thru 2A3Z6		SAME AS 2A1Z1.	5-14
2A3Z7		INTEGRATED CIRCUIT, DIGITAL AND GATE: 11 pins, plastic case; supply voltage, -12 v, 0.1875 in. lg by 0.625 in. wd by 0.438 in. hg. 82679 P/N NW142-24.	5-14
2A3Z8		SAME AS 2A1Z1.	5-14
2A3Z9		SAME AS 2A1Z6.	5-14
2A3Z10		SAME AS 2A1Z1.	5-14
2A3Z11		SAME AS 2A1Z6.	5-14
2A3Z12		INTEGRATED CIRCUIT, DIGITAL AND GATE: 11 pins, plastic case; supply voltage, -12 v. 0.875 in. lg by 0.625 in. wd by 0.438 in. hg. 82679 P/N NW142-34.	5-14

TABLE 6-2. MAINTENANCE PARTS LIST (Continued)

CHANNEL/FREQUENCY INDICATOR, RTIH-3

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
2A3Z13		SAME AS 2A3Z12.	5-14
2A3Z14		INTEGRATED CIRCUIT, DIGITAL NOR GATE: 11 pins, plastic case; supply voltage + and -12 v. 0.875 in. lg by 0.625 in. wd by 0.438 in. hg. 82679 P/N NW145-61.	5-14
2A4		CIRCUIT CARD ASSEMBLY: 15 integrated circuits, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4495.	5-16
2A4Z1 thru 2A4Z3		SAME AS 2A3Z12.	5-16
2A4Z4 thru 2A4Z15		SAME AS 2A1Z1.	5-16
2A5		SAME AS 2A4.	5-16
2A6		CIRCUIT CARD ASSEMBLY: 12 integrated circuits, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4493.	5-18
2A6Z1 thru 2A6Z8		SAME AS 2A1Z1.	5-18
2A6Z9		SAME AS 2A3Z7.	5-18
2A6Z10		INTEGRATED CIRCUIT, DIGITAL POSITIVE EMITTER FOLLOWER: 12 pins, plastic case; -6 vdc input, -6.7 output. 0.865 in. lg by 0.678 in. wd by 0.495 in. hg. 82679 P/N NW148-4.	5-18 5-18
2A6Z11		SAME AS 2A6Z10.	5-18
2A6Z12		SAME AS 2A3Z7.	5-18
2A7		SAME AS 2A6.	5-18
2A8		CIRCUIT CARD ASSEMBLY: 1 resistor, 2 capacitors, 14 integrated circuits; plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4530.	5-20
2A8C1		CAPACITOR, FIXED, MICA: 3,900 uuf, ±2% tol, 500 vdcw, 0.680 in. lg by 0.540 in. wd by 0.270 in. thk. 82679 P/N CM112F392G5S.	5-20
2A8C2		CAPACITOR, FIXED, MICA: 1,000 uuf, ±1% tol, 100 vdcw, 0.790 in. lg by 0.570 in. wd by 0.340 in. thk. 82679 P/N CM111F102F1S.	5-20
2A8R1		SAME AS 2A2R1.	5-20
2A8Z1		INTEGRATED CIRCUIT, DIGITAL AND GATE: 11 pins, plastic case; supply voltage, -12 v. 0.875 in. lg by 0.625 in. wd by 0.438 in. hg. 82679 P/N NW141-91.	5-20
2A8Z2 thru 2A8Z6		SAME AS 2A1Z1.	5-20
2A8Z7		INTEGRATED CIRCUIT, DIGITAL, SINGLE SHOT GENERATOR: 11 pins, plastic case; supply voltage, + and -12 v. 0.875 in. lg by 0.625 in. wd by 0.438 in. hg. 82679 P/N NW153.	5-20

TABLE 6-2. MAINTENANCE PARTS LIST (Continued)

CHANNEL/FREQUENCY INDICATOR, RTIH-3

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
2A8Z8		INTEGRATED CIRCUIT, COMPLEMENTARY EMITTER FOLLOWER: 11 pins, plastic case; supply voltage; -12 v 0.875 in. lg by 0.625 in. wd by 0.438 in. hg. 82679 P/N NW147-2.	5-20
2A8Z9		SAME AS 2A6Z10.	5-20
2A8Z10		SAME AS 2A1Z1.	5-20
2A8Z11 thru 2A8Z14		SAME AS 2A6Z10.	5-20
2A9		CIRCUIT CARD ASSEMBLY: 5 resistors, 3 capacitors, 10 integrated circuits, 4 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4496.	5-22
2A9C1		CAPACITOR, FIXED, PLASTIC: 1.8 uf, ±5% tol, 0.656 in. dia by 1.250 in. lg. 82679 P/N CN112A185J.	5-22
2A9C2		SAME AS 2A9C1.	5-22
2A9C3		CAPACITOR, FIXED, MICA: 1500 pf, ±1% tol, 500 vdcw. 0.440 in. lg by 0.473 in. wd by 0.170 in. thk. 82679 P/N CM112F152F5S.	5-22
2A9CR1		SEMICONDUCTOR DEVICE: MIL type 1N914.	5-22
2A9CR2		SAME AS 2A9CR1.	5-22
2A9CR3		SAME AS 2A9CR1.	5-22
2A9CR4		SAME AS 2A9CR1.	5-22
2A9R1		RESISTOR, VARIABLE, WIRE WOUND: 500 ohms, ±10% tol, 1/2 watt. 1.250 in. lg by 0.250 in. wd by 0.313 in. hg. wire lead mounted. 82679 P/N RV121-1-501.	5-22
2A9R2		RESISTOR: MIL type RC07GF472J.	5-22
2A9R3		RESISTOR: MIL type RC07GF122J.	5-22
2A9R4		SAME AS 2A9R3.	5-22
2A9R5		RESISTOR: MIL type RC32GF331J.	5-22
2A9Z1		INTEGRATED CIRCUIT, DIGITAL TIMING GENERATOR: 11 pins, plastic case; -8 v output voltage. 0.895 in. lg by 0.678 in. wd by 0.495 in. hg. 82679 P/N NW152.	5-22
2A9Z2		SAME AS 2A1Z1.	5-22
2A9Z3		INTEGRATED CIRCUIT, DIGITAL DUAL INVERTER: 11 pins, plastic case; supply voltage, + an -12 v. 0.875 in. lg by 0.625 in. wd by 0.438 in. hg. 82679 P/N NW150-2.	5-22
2A9Z4		SAME AS 2A8Z7.	5-22
2A9Z5		SAME AS 2A1Z1.	5-22
2A9Z6		SAME AS 2A1Z1.	5-22
2A9Z7		SAME AS 2A1Z1.	5-22
2A9Z8		INTEGRATED CIRCUIT, DIGITAL AND GATE: 11 pins, plastic case; supply voltage, -12 v. 0.875 in. lg by 0.625 in. wd by 0.438 in. hg. 82679 P/N NW142-43.	5-22
2A9Z9		SAME AS 2A9Z8.	5-22
2A9Z10.		SAME AS 2A8Z8.	5-22
2A10		CIRCUIT CARD ASSEMBLY: 17 resistors, 4 capacitors, 2 integrated circuits, 4 transistors, 2 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4545.	5-24
2A10C1		CAPACITOR: MIL type CS13BF475K.	5-24
2A10C2		SAME AS 2A10C1.	5-24
2A10C3		CAPACITOR, FIXED, MICA: 47 uuf, ±2% tol, 500 vdcw. 0.440 in. lg by 0.473 in. wd by 0.170 in. thk. 82679 P/N CM11E470G5S.	5-24
2A10C4		SAME AS 2A10C3.	5-24
2A10CR1		RECTIFIER, SEMICONDUCTOR DEVICE: Peak reverse v, 260 v, 1.50 vdc output current, 0.688 in. wd by 0.469 in. hg by 0.250 in. thk. 82679 P/N DD130-200-1.5.	5-24

TABLE 6-2. MAINTENANCE PARTS LIST (Continued)

CHANNEL/FREQUENCY INDICATOR, RTIH-3

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
2A10CR2		RECTIFIER, SEMICONDUCTOR DEVICE: 1.5 vdc output current, peak reverse v, 600 v. 0.688 in. hg by 0.250 in. thk. 82679 P/N DD130-600-1.5.	5-24
2A10Q1		TRANSISTOR: MIL type 2N1485.	5-24
2A10Q2		TRANSISTOR: MIL type 2N4036.	5-24
2A10Q3		SAME AS 2A10Q1.	5-24
2A10Q4		SAME AS 2A10Q2.	5-24
2A10R1		RESISTOR: MIL type RC20GF680J.	5-24
2A10R2		RESISTOR: MIL type RC20GF560J.	5-24
2A10R3		RESISTOR: MIL type RNG0D1802D.	5-24
2A10R4		RESISTOR: MIL type RC20GF471J.	5-24
2A10R5		RESISTOR: MIL type TC60D2711D.	5-24
2A10R6		RESISTOR: MIL type RC42GF101J.	5-24
2A10R7		SAME AS 2A9R5.	5-24
2A10R8		RESISTOR: MIL type RC32GF104J.	5-24
2A10R9		SAME AS 2A10R3.	5-24
2A10R10		SAME AS 2A10R5.	5-24
2A10R11		SAME AS 2A10R1.	5-24
2A10R12		SAME AS 2A10R2.	5-24
2A10R13		RESISTOR: MIL type RC20GF561J.	5-24
2A10R14		RESISTOR, FIXED, WIRE WOUND: 3 ohms, ±5% tol, 5 watts. 0.250 in. dia by 1.000 in. lg, wire lead mounted. 82679 P/N RR114-3R0W.	5-24
2A10R15		SAME AS 2A2R6.	5-24
2A10R16		RESISTOR: MIL type RC20GF1R0J.	5-24
2A10R17		SAME AS 2A10R16.	5-24
2A10Z1		VOLTAGE REGULATOR: 40 v input, 30 v output, 400 mw power dissipation. 0.330 in. dia by 0.175 in. lg. 82679 P/N VR104.	5-24
2A14		CIRCUIT CARD ASSEMBLY: 4 capacitors, 9 integrated circuits, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4625.	5-26
2A14C1		SAME AS 2A1C1.	5-26
2A14C2		SAME AS 2A1C1.	5-26
2A14C3		SAME AS 2A1C1.	5-26
2A14C4		SAME AS 2A1C1.	5-26
2A14Z1		SAME AS 2A1Z1.	5-26
2A14Z2		SAME AS 2A1Z1.	5-26
2A14Z3		SAME AS 2A1Z1.	5-26
2A14Z4		SAME AS 2A3Z7.	5-26
2A14Z5		SAME AS 2A3Z7.	5-26
2A14Z6		SAME AS 2A1Z1.	5-26
2A14Z7		SAME AS 2A3Z12.	5-26
2A14Z8		SAME AS 2A1Z6.	5-26
2A14Z9		SAME AS 2A1Z6.	5-26
2A15		SAME AS 2A14.	5-26
2A16		SAME AS 2A1.	

TABLE 6-2. MAINTENANCE PARTS LIST (Continued)

ELECTRONIC COMMAND SIGNAL PROGRAMMER, RTPH-3

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
3		RTPH-3, PROGRAMMER, ELECTRONIC COMMAND SIGNAL C-7775/UR: Model RTPH-3 allows one control location to take command over many receiver systems. Instructions are programmed by means of pushbuttons on the front of the unit. By various codes, systems are selected and their frequency tuned over a 2 to 32 m range, accuracy to 100 cycles. Signal mode, AGC Time Constant are at the command of the control panel; selection of symmetrical mode, cw or independent sideband operation can be set by the RTPH unit.	1-1
3A1		CIRCUIT CARD ASSEMBLY: 22 resistors, 7 capacitors, 2 integrated circuits, 3 transistors, 2 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4601.	5-30
3A2		CIRCUIT CARD ASSEMBLY: 7 resistors, 2 capacitors, 1 relay, 2 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82670 P/N A4516.	5-30
3A3		CIRCUIT CARD ASSEMBLY: 2 resistors, 2 capacitors, 9 integrated circuits, 1 coil, 2 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4518.	5-30
3A4		CIRCUIT CARD ASSEMBLY: 1 resistor, 2 integrated circuits, 5 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4598.	5-30
3A5		CIRCUIT CARD ASSEMBLY: 80 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.375 in. hg. 82679 P/N A4453.	5-30
3A6		SWITCH ASSEMBLY: 3 banks of 15 ea pushbutton switches. 3.125 in. hg by 11.125 in. wd by 3.750 in. deep. 82679 P/N SW479.	5-30
3C1		CAPACITOR, FIXED, ELECTROLYTIC: 2600 uf, 50 vdcw. 1.438 in. dia by 3.500 in. lg. Dwg CE112-6, 80183 36D262G050AB6B.	5-31
3C2		SAME AS 3C1.	5-31
3DS1		LAMP INCANDESCENT: Single contact, T-1-3/4 base, 28 vac or dc, 0.04 amps. Dwg BI110-10, 08806 P/N 327.	5-28
3F1		FUSE CARTRIDGE TYPE: Lamp 125 v. 0.250 in. dia by 1.250 in. lg. Dwg FU102-1, 71400 P/N MDL-1.	5-28
3F2		SAME AS 3F1.	5-28
3FL1		FILTER, RADIO INTERFERENCE: Current 5 amps; voltage rating, 500 vdc; 250 vac at 60 cps. 1.000 in. dia by 2.688 in. lg. Dwg FI105-2, 80183 P/N 5JX100.	5-30
3FL2		SAME AS 3FL1.	5-30
3J1		CONNECTOR: MIL type MS3102A14S1P.	5-29
3J2		CONNECTOR: MIL type MS3102A20-27P.	5-29
3Q1		TRANSISTOR: MIL type 2N3055.	5-30
3R1		RESISTOR: MIL type RC32GR101J.	5-31
3S1		SWITCH: MIL type ST22K.	5-28
3T1		TRANSFORMER, POWER, STEP DOWN: Primary, 115/230 v, 50/60 hz, 1 phase. Secondary, 18 v, 30 madc; 20 v, 200 madc; 18 v, 2 adc. Hermetically sealed metal case, stud mtd. 3.875 in. hg by 3.937 in. lg by 3.375 in. wd. 82679 P/N TF376.	5-30
3XA1		CONNECTOR, RECEPTACLE, ELECTRICAL: 22 double sided female contacts rated at 5 amps and 1800 volts, rms, phenolic housing with floating bushing and eyelet terminals. Accepts printed circuit board thickness of 0.054 in. to 0.071 in. 82679 P/N JJ319-22-DFE.	5-31

TABLE 6-2. MAINTENANCE PARTS LIST (Continued)

ELECTRONIC COMMAND SIGNAL PROGRAMMER, RTPH-3

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
3XA2 thru 3XA5		SAME AS 3XA1.	5-31
3XDS1		LIGHT, INDICATOR: Translucent white lens. 1.35 to 28 v T-1-3/4 lamp base. 2 terminals. 0.437 in. dia by 1.500 in. lg. Dwg TS153-12, 72619 P/N 162-8430-1475-502.	5-28
3XF1		FUSEHOLDER, LAMP INDICATING: 90-250 v, 15 amps, neon lamp, clear knob, accommodates 1/4 in. dia by 1-1/4 in. lg fuse. Dwg FH104-3, 71400 P/N HKL-X.	5-28
3XF2		SAME AS 3XF1.	5-28
3XQ1		SOCKET, SEMICONDUCTOR DEVICE: 2 pin contact accommodation, 0.040 in. or 0.050 in. dia; polarized; 1 terminal lug grounding strap; 1.578 in. lg, 1.000 in. wd 0.172 in. thk. Dwg TS166-1, 91506.P/N 8038-1G1.	5-30
3A1		CIRCUIT CARD ASSEMBLY: 22 resistors, 7 capacitors, 2 integrated circuits, 3 transistors, 2 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4601.	5-33
3A1C1		CAPACITOR, FIXED, ELECTROLYTIC: 4.7 uf, 10% tol, 35 vdcw, 0.175 in. dia by 0.438 in. lg. 82679 P/N CE123-475-35B2.	5-33
3A1C2		SAME AS 3C1.	5-33
3A1C3		CAPACITOR, FIXED, ELECTROLYTIC: 100 uf, ±10% tol, 20 vdcw, 0.341 ind dia by 6.750 in. lg. 82679 P/N CE123-107-20S2.	5-33
3A1C4		CAPACITOR, FIXED, MICA: 47 uuf, ±2% tol, 500 vdcw. 0.440 in. lg by 0.473 in. wd by 0.170 in. thk. 82679 P/N CM111F470G5S.	5-33
3A1C5		SAME AS 3A1C4.	5-33
3A1C6		CAPACITOR, FIXED, CERAMIC: 10,000 uuf, +80% -20% tol, 25 vdcw; 0.385 in. dia by 0.156 in. thk, 0.250 in. lead spacing. 82679 P/N CC100-41.	5-33
3A1C7		SAME AS 3A1C6.	5-33
3A1CR1		RECTIFIER, SEMICONDUCTOR DEVICE: Peak reverse v, 260 v. -0.688 in. wd, 0.469 in. hg, 0.250 in. thk. 82679 P/N DD130-200-1.5.	5-33
3A1CR2		RECTIFIER, SEMICONDUCTOR DEVICE: 200 piv; plastic case, 4 wire lead mtd. 0.750 in. lg by 0.750 in. wd by 0.438 in. hg. 82679 P/N DD143-27.	5-33
3A1Q1		TRANSISTOR: MIL type 2N1485.	5-33
3A1Q2		TRANSISTOR: MIL type 2N4036.	5-33
3A1Q3		SAME AS 3A1Q2.	5-33
3A1R1		RESISTOR: MIL type RC20GF680J.	5-33
3A1R2		RESISTOR: MIL type RC20GF560J.	5-33
3A1R3		RESISTOR: MIL type RC20GF561J.	5-33
3A1R4		RESISTOR: MIL type RN60D2711D.	5-33
3A1R5		RESISTOR: MIL type RN60D1802D.	5-33
3A1R6		RESISTOR, FIXED, WIRE WOUND: 3 ohms, ±5% tol, 5 watts, 0.250 in. dia by 1.000 in. lg, wire lead mounted. 82679 P/N RR114-3W.	5-33
3A1R7		RESISTOR: MIL type RC20GF1R0J.	5-33
3A1R8		SAME AS 3A1R7.	5-33
3A1R9		RESISTOR: MIL type RC32GF271J.	5-33
3A1R10		RESISTOR: MIL type RC20GF272J.	5-33
3A1R11		RESISTOR: MIL type RC20GF122J.	5-33
3A1R12		SAME AS 3A1R5.	5-33
3A1R13		SAME AS 3A1R4.	5-33
3A1R14		RESISTOR, FIXED, WIRE WOUND: 1 ohm, ±5% tol, 5 watts. 0.250 in. dia by 1.000 in. lg, wire lead mounted. 82679 P/N RR114-1W.	5-33

TABLE 6-2. MAINTENANCE PARTS LIST (Continued)

ELECTRONIC COMMAND SIGNAL PROGRAMMER, RTPH-3

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
3A1R15		SAME AS 3A1R1.	5-33
3A1R16		SAME AS 3A1R2.	5-33
3A1R17		RESISTOR: MIL type RC20GF361J.	5-33
3A1R18		RESISTOR: MIL type RC42GF271J.	5-33
3A1R19		SAME AS 3A1R7.	5-33
3A1R20		SAME AS 3A1R7.	5-33
3A1R21		SAME AS 3A1R7.	5-33
3A1R22		SAME AS 3A1R7.	5-33
3A1Z1		VOLTAGE REGULATOR: 40 v input, 30 v output, 400 mw dissipation. 0.330 in. dia by 0.175 in. lg. 82679 P/N VR104.	5-33
3A1Z2		SAME AS 3A1Z1.	5-33
3A2		CIRCUIT CARD ASSEMBLY, 7 resistors, 2 capacitors, 1 relay, 2 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4516.	5-35
3A2C1		CAPACITOR, FIXED, MICA: 1,000 uuf, ±5% tol, 100 vdcw, 0.640 in. lg, 0.591 in. wd by 0.198 in. thk. 82679 P/N CM111F102J1S.	5-35
3A2C2		SAME AS 3A2C1.	5-35
3A2CR1		SEMICONDUCTOR: MIL type 1N4245.	5-35
3A2CR2		SAME AS 3A2CR1.	5-35
3A2K1		RELAY, ARMATURE: Mercury wetted contacts rated at 2 amps max, 500 v max. 2 windings rated at 250 ohms each ±10%. 2.063 in. lg by 0.625 in. hg by 0.625 in. wd, wire lead mounted. 82679 P/N RL167-1.	5-35
3A2R1		RESISTOR: MIL type RC20GF471J.	5-35
3A2R2		RESISTOR: MIL type RC20GF681J.	5-35
3A2R3		SAME AS 3A2R2.	5-35
3A2R4		RESISTOR: MIL type RC20GF4R7J.	5-35
3A2R5		SAME AS 3A2R4.	5-35
3A2R6		RESISTOR: MIL type RC20GF101J.	5-35
3A2R7		SAME AS 3A2R6.	5-35
3A3		CIRCUIT CARD ASSEMBLY: 2 resistors, 2 capacitors, 9 integrated circuits, 1 coil, 2 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4518.	5-37
3A3C1		CAPACITOR, FIXED, PLASTIC: 1.8 uf, ±5% tol. 0.406 in. dia by 0.813 in. lg. 82679 P/N CN112A185J.	5-37
3A3C2		SAME AS 3A3C1.	5-37
3A3CR1		SEMICONDUCTOR: MIL type 1N914.	5-37
3A3CR2		SAME AS 3A3CR1.	5-37
3A3L1		COIL, RF, FIXED: 1000 uh, ±10%, 17.5 ohms max dc res. 0.157 dia, 0.450 in. lg. 82679 P/N CL275-102.	5-37
3A3R1		RESISTOR, VARIABLE, WIRE WOUND: 500 ohms, ±10% tol, 1/2 watt. 1.250 in. lg by 0.250 in. wd by 0.313 in. hg, wire lead mounted. 82679 P/N RV121-1-501.	5-37
3A3R2		RESISTOR: MIL type RC07GF122J.	5-37
3A3Z1		INTEGRATED CIRCUIT, DIGITAL TIMING GENERATOR: 11 pins, plastic case; -8 v output voltage. 0.895 in. lg by 0.678 in. wd by 0.495 in. hg. 82679 P/N NW152.	5-37
3A3Z2		INTEGRATED CIRCUIT, DIGITAL FLIP FLOP: 11 pins, plastic case; -4.5 v input voltage, -9.5 v output voltage. 0.895 in. lg by 0.678 in. wd by 0.495 in. hg. 82679 P/N NW151.	5-37
3A3Z3		SAME AS 3A3Z2.	5-37
3A3Z4		SAME AS 3A3Z2.	5-37

TABLE 6-2. MAINTENANCE PARTS LIST (Continued)

ELECTRONIC COMMAND SIGNAL PROGRAMMER, RTPH-3

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
3A3Z5		SAME AS 3A3Z2.	5-37
3A3Z6		INTEGRATED CIRCUIT, DIGITAL AND GATE: 11 pins, plastic case; supply voltage, -12 v. 0.875 in. lg by 0.625 in. wd by 0.438 in. hg. 82679 P/N NW141-42.	5-37
3A3Z7		SAME AS 3A3Z6.	5-37
3A3Z8		SAME AS 3A3Z6.	5-37
3A3Z9		INTEGRATED CIRCUIT, DIGITAL NOR GATE: 11 pins, plastic case; supply voltage, + and - 12 v. 0.875 in. lg by 0.625 in. wd by 0.438 in. hg. 82679 P/N NW145-61.	5-37
3A4		CIRCUIT CARD ASSEMBLY: 1 resistor, 2 integrated circuits, 5 semiconductors, plug-in item; 4.375 in. lg by 4.125 in. wd by 0.750 in. hg. 82679 P/N A4598.	5-39
3A4CR1 thru 3A4CR5		SAME AS 3A3CR1.	5-39
3A4R1		RESISTOR: MIL type RC07GF681J.	5-39
3A4Z1		INTEGRATED CIRCUIT, DIGITAL DUAL INVERTER: 11 pins, plastic case; supply voltage, + and -12 v. 0.875 in. lg by 0.625 in. wd by 0.438 in. hg. 82679 P/N NW150-2.	5-39
3A4Z2		SAME AS 3A3Z2.	5-39
3A5		CIRCUIT CARD ASSEMBLY: 80 semiconductors, plug-in item, 4.375 in. lg by 4.125 in. wd by 0.375 in. hg. 82679 P/N A4453.	5-41
3A5CR1 thru 3A5CR80		SAME AS 3A3CR1.	5-41
3A6		SWITCH ASSEMBLY: 3 banks of 15 each pushbutton switches. 3.125 in. hg by 11.125 in. wd by 3.750 in. deep. 82679 P/N SW479.	5-28
3A6MP		PUSHBUTTONS: 0.438 in. lg by 0.438 in. wd by 0.625 in. deep. 3A6MP( ) series listed below. 82679 P/N HB-127 series.	5-28
3A6MP1		PUSHBUTTON, Blank, bluc, HB127-1.	5-28
3A6MP2		PUSHBUTTON, Blank, yellow, HB127-2.	5-28
3A6MP3		PUSHBUTTON, Engraved "TUNE", green, HB127-3.	5-28
3A6MP4		PUSHBUTTON, Engraved "CLEAR", red, HB127-4.	5-28
3A6MP5		PUSHBUTTON, Engraved "10 MC", yellow, HB127-5.	5-28
3A6MP6		PUSHBUTTON, Engraved "1 MC", yellow, HB127-6.	5-28
3A6MP7		PUSHBUTTON, Engraved "100 KC", yellow, HB127-7.	5-28
3A6MP8		PUSHBUTTON, Engraved "10 KC", yellow, HB127-8.	5-28
3A6MP9		PUSHBUTTON, Engraved "1 KC", yellow, HB127-9.	5-28
3A6MP10		PUSHBUTTON, Engraved ".1 KC", yellow, HB127-10.	5-28
3A6MP11		PUSHBUTTON, Engraved "MODE", yellow, HB127-11.	5-28
3A6MP12		PUSHBUTTON, Engraved "SYN/B2", yellow, HB127-12.	5-28
3A6MP13		PUSHBUTTON, Engraved "B1", yellow, HB127-13.	5-28
3A6MP14		PUSHBUTTON, Engraved "A1", yellow, HB127-14.	5-28
3A6MP15		PUSHBUTTON, Engraved "A2", yellow, HB127-15.	5-28
3A6MP16		PUSHBUTTON, Engraved "FUNC", yellow, HB127-16.	5-28
3A6MP17		PUSHBUTTON, Engraved "A", black, HB127-17.	5-28
3A6MP18		PUSHBUTTON, Engraved "B", black, HB127-18.	5-28
3A6MP19		PUSHBUTTON, Engraved "C", black, HB127-19.	5-28
3A6MP20		PUSHBUTTON, Engraved "D", black, HB127-20.	5-28
3A6MP21		PUSHBUTTON, Engraved "E", black, HB127-21.	5-28

TABLE 6-2. MAINTENANCE PARTS LIST (Continued)

ELECTRONIC COMMAND SIGNAL PROGRAMMER, RTPH-3

REF DESIG	NOTES	NAME AND DESCRIPTION	FIG. NO.
3A6MP22		PUSHBUTTON, Engraved "1", white, HB127-22.	5-28
3A6MP23		PUSHBUTTON, Engraved "2", white, HB127-23.	5-28
3A6MP24		PUSHBUTTON, Engraved "3", white, HB127-24.	5-28
3A6MP25		PUSHBUTTON, Engraved "4", white, HB127-25.	5-28
3A6MP26		PUSHBUTTON, Engraved "5", white, HB127-26.	5-28
3A6MP27		PUSHBUTTON, Engraved "6", white, HB127-27.	5-28
3A6MP28		PUSHBUTTON, Engraved "7", white, HB127-28.	5-28
3A6MP29		PUSHBUTTON, Engraved "8", white, HB127-29.	5-28
3A6MP30		PUSHBUTTON, Engraved "9/A", white, HB127-30.	5-28
3A6MP31		PUSHBUTTON, Engraved "10/B", white, HB127-31.	5-28
ELECTRICAL EQUIPMENT CABINET, C0N102BJ			
4		C0N102BJ, CABINET, ELECTRICAL EQUIPMENT (CY-6538/URA-63) is a cabinet specially designed to house the components of the Console, Communications Control, AN/URA-63.	5-1
4DS1		LAMP, FLUORESCENT: 115/125 v ac, 30 watts, frosted glass. 1.000 in. dia by 17.750 in. lg. Dwg no. BI108, 26042 P/N L30/IF.	5-42
4DS2		SAME AS 4DS1.	5-42
4J1		CONNECTOR, RECEPTACLE, ELECTRICAL: 15 amp, 125 v, 3 wire grounding. Dwg no. JJ337, 79725 P/N 2127GA.	5-42
4J2		SAME AS 4J1.	5-42
4J3		SAME AS 4J1.	5-42
4J4		SAME AS 4J1.	5-42
4S1		SWITCH: MIL type ST22K.	5-42
4XDS1		SOCKET, FLUORESCENT LAMP: 660 watts, 250 v ac, black phenolic body. 1.375 in. lg by 0.812 in. wd by 0.812 in. hg. 82679 P/N TS145.	5-42
4XDS2		SAME AS 4XDS1.	5-42

TABLE 6-3. LIST OF MANUFACTURERS

MFR CODE	NAME	ADDRESS
08806	General Electric Company Miniature Lamp. Dept.	Nela Park Cleveland, Ohio 44112
14655	Cornell-Dublier Electronics Div. Federal Pacific Electric Co.	50 Paris Street Newark, New Jersey 07105
71400	Bussmann Mfg. Division of McGraw & Edison Co.	2536 W. University St. St. Louis, Mo. 63017
72619	Dialight Corp.	60 Steward Avenue Brooklyn, N. Y. 11237
72983	Essex Wire Corp.	1601 Wall Street Fort Wayne, Ind. 46804
75382	Kulka Electric Corp.	520 S. Fulton Ave. Mt. Vernon, N. Y. 10550
80183	Sprague Products Co.	North Adams Massachusetts
81349	Military Specifications Promulgated By Standardization Div.	Directorate of Logistic Services DSA
82679	The Technical Materiel Corp.	700 Fenimore Road Mamaroneck, N. Y. 10543
83594	Burroughs Corp. Electronic Components Div.	P. O. Box 1226 Plainfield, N. J. 07061
91506	Augat Inc.	33 Perry Avenue Attleboro, Mass. 02703

INDEX

INDEX (Cont)

INDEX (Cont)

NAVELEX NO. 0967-385-1010

USER ACTIVITY COMMENT SHEET

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