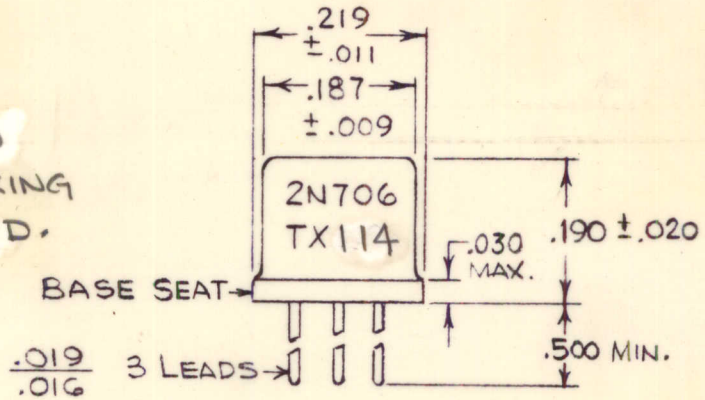
STANDARD DRAWING

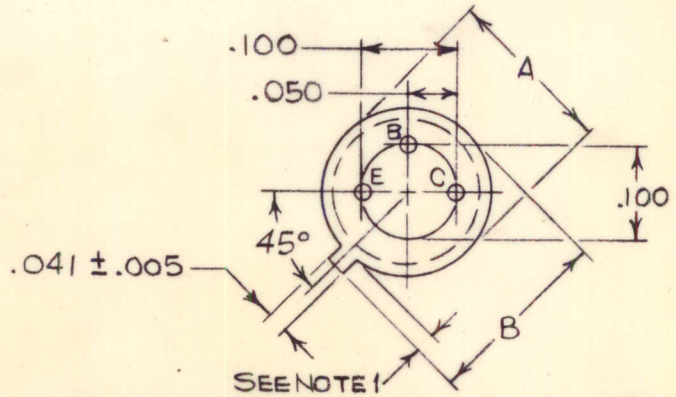
REQ. PER UNIT	USED ON MODEL	ASS'Y. NO.	DATE	TX114	Ø
	CDN-3				

h_{FE} LIMITS 70 MIN
TEST CONDITIONS
V_{CE} = 1 V
I_C = 10MA.

TX114 IS A JEDEC TYPE 2N706 SILICON NPN TRANSISTOR WITH A CONTROLLED h_{FE}. THE CASE SHALL BE JEDEC TYPE TO-18.

NOTE 2:
CASE SHALL BE MARKED AS SHOWN OR THE MARKING "2N706" MAY BE OMITTED.





NOTE 1:
TAB LENGTH TO BE .028 MIN.-.048 MAX. AND WILL BE DETERMINED BY SUBTRACTING DIA. "A" FROM DIMENSION "B".

SYM	DESCRIPTION	DATE	CH. NO.	DRAFTS	CHECKER	ENG. APP.
Ø	ORIGINAL RELEASE	3/1/66	Ø			

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

DECIMALS .X ±.05 .XX ±.01 .XXX ±.005 TOLERANCES FRACTIONS ± 1/64 ANGLES ± 0° 30'

SCALE

CODE C

S401-424

REQ.	ITEM	PART NO.	DESCRIPTION	SYMBOL

STOCK SIZE

THE TECHNICAL MATERIEL CORP.
MAMARONECK. NEW YORK

MATERIAL

TRANSISTOR, SILICON, NPN
2N706

TYPE & TEMPER | HEAT TREAT. SPEC.

DRAWN	CHECKED	FINAL APPROVAL
JAD	2/23/66	

FINISH & SPEC. NO.

ELEC. DES. APP.	MECH. DES. APP.	TX114	Ø

TMC FORM 108-A

REPROVEL NO. 440H 23848