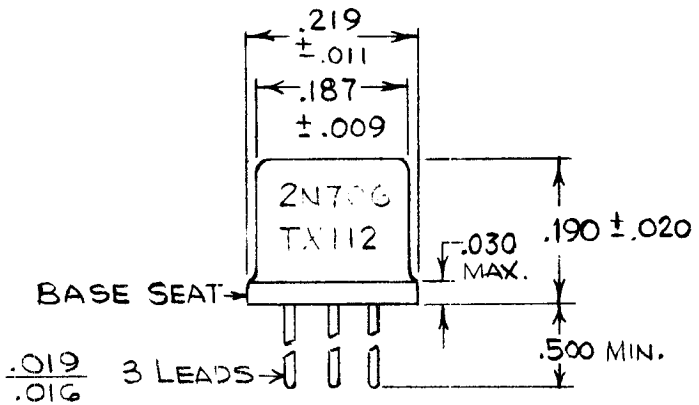
STANDARD DRAWING

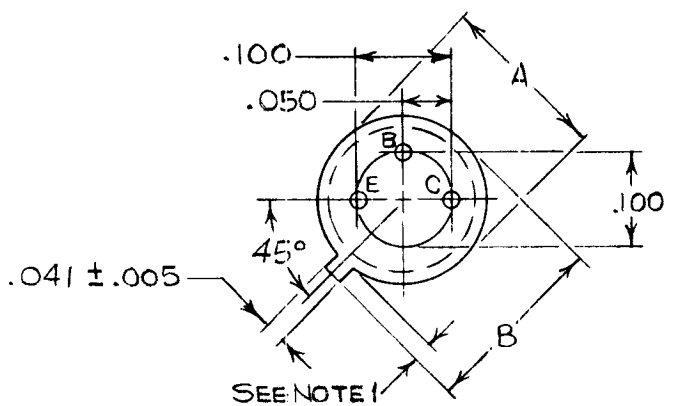
REQ. PER UNIT	USED ON MODEL	USED ON ASS'Y. NO.	USED ON DATE	TX112	Ø

h_{FE} LIMITS 40-60
TEST CONDITIONS
$V_{CE} = 1V$
$I_C = 10mA$

TX112 IS A JEDEC TYPE 2N706 SILICON NPN TRANSISTOR WITH A CONTROLLED h_{FE}. THE CASE SHALL BE JEDEC TYPE TO-18.

NOTE 2:
CASE SHALL BE MARKED AS SHOWN OR THE MARKING "2N706" MAY BE OMITTED.





NOTE 1:
TAB LENGTH TO BE .028 MIN. .048 MAX. AND WILL BE DETERMINED BY SUBTRACTING DIA. "A" FROM DIMENSION "B".

SYM	DESCRIPTION	DATE	CH. NO.	DRAFTS	CHECKER	ENG. APP.
Ø	ORIGINAL RELEASE FOR PRODUCTION	6-17-65	—	JC		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

SCALE —

DECIMALS .X ±.05 .XX ±.01 .XXX ±.005 — TOLERANCES — FRACTIONS ± 1/64 ANGLES ± 0° 30'

CODE C

S401-40

REQ.	ITEM	PART NO.	DESCRIPTION	SYMBOL
		—		

STOCK SIZE —

MATERIAL —

TYPE & TEMPER — HEAT TREAT. SPEC. —

FINISH & SPEC. NO. —

THE TECHNICAL MATERIEL CORP.
MAMARONECK. NEW YORK

TRANSISTOR, SILICON, NPN
2N706

DRAWN	CHECKED	FINAL APPROVAL
H. AUSTIN	JC 6-17-65	

ELEC. DES. APP.	MECH. DES. APP.	TX112	Ø

TMC FORM 108-A

REPROVEL NO. 440H 23645