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CONFIGURATION ITEM VERIFICATION REVIEW (CIVR) VALIDATION REPORT

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TMC F RM SPEC 1 2M 9-45-AIN

g) SMA 595922 REQUIREMENTS FOR CIRCUIT CARD ASSEMBLIES

f) TMC SPECIFICATION S1394

-	TMC SPECIFICATION												NO. S1412															
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1. PURPOSE:

TO ASSURE THAT THE PARTS, MATERIALS AND PROCESSES USED IN SM-D-586702 ASSEMBLY ARE THOSE SPECIFIED ON THE GOVERNMENT FURNISHED DRAWINGS OR SPECIFICATIONS.

2. COMPLIANCE

ALL COMPONENTS USED IN THE MANUFACTURE OF SM-D-586702 (TARGET ADDER ASSEMBLY) MEET THE REQUIREMENTS AND STATED ON DRAWING PL SM-B-586702. FOR EACH COMPONENT USED A CERTIFICATE OF COMPLIANCE IS AVAILABLE ALONG WITH TMC'S PURCHASE ORDER ON ALL MATERIALS.

3. INCOMING MATERIAL CONTROL PROCEDURES

ALL MATERIAL IS COMPARED WITH THE RECEIVING REPORT. VERIFICATION OF VENDOR, QUANTITIES, PART NUMBERS AND ACCURACY OF CERTIFICATES OF COMPLIANCE IS REVIEWED.

BEFORE MATERIALS ARE ISSUED ON THE PRODUCTION FLOOR A SAMPLING TEST OF MATERIALS PERFORMED.

3. a. PRINTED WIRING BOARD SM-D-586602 WAS INSPECTED IN ACCORDANCE WITH GOVERNMENT SUPPLIED DRAWINGS (SM-D-586602) SHEETS 1, 2 AND 3) ALSO MIL-STD-252B PAGES 15, 16 AND 17.

CAPACITORS C1 AND C2 HAVE BEEN INSPECTED USING THE INSPECTION METHOD (REF. MIL-STD-105) TMC STANDARD QA3008.

M21097/15-13 (P1) CONNECTOR WAS INSPECTED, USING AS A GUIDE AMP SPECIAL INDUSTRIES PRODUCT BULLETIN 703-3 PRINTED CIRCUIT & ELECTRONIC PACKAGING PRODUCTS.

CONNECTOR SM-D-586461 WAS INSPECTED IN ACCORDANCE WITH THE GOVERNMENT SUPPLIED DRAWING SM-D-586461.

ALL THE INTERGRATED CIRCUITS U1 THROUGH U14 WERE EXAMINED, USING THE INSPECTION METHOD REF. (MIL STANDARD 105) TMC STANDARD QA3008 AND MIL STANDARD 454 REQUIREMENT 64.

TMC SPECIFICATION NO. S1412 REV: APPD: SHEET OF	
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TITLE: Configuration Item Verification Review CIVR Validation Report	

4. ASSEMBLING PROCEDURE

ALL COMPONENT PARTS FOR THE (TARGET ADDER ASSEMBLY) ASSEMBLED AS PER DRAWING SM-D-586702. ALL COMPONENTS ARE HAND SOLDERED IN ACCORDANCE WITH MIL STD 454 REQUIREMENT 5, AND THE METHOD OF ASSEMBLY CONFORMS WITH "GENERAL REQUIREMENTS FOR CIRCUIT CARD ASSEMBLIES" SM-A-595922.

5. MARKING PROCESS

MARKING PROCESS CONFORMS TO MIL-M-13231A, AS NOTED ON ASSEMBLY DRAWING SM-D-586702, NOTE 4.

6. CONFORMAL COATING

PROTECTIVE COATING PROCESS CONFIRMS TO SM-A-587204 AND TMC SPECIFICATION S1394.

TMC SPECIFICATION

REV: NO. S1412

COMPILED: R. UZZO CHECKED: APPD: SMEET OF

TITLE: Configuration Item Verification Review CIVR Validation Report

7. CONTRACTOR TESTING

FIRST ARTICLE APPROVAL CONTRACTOR TESTING WAS PERFORMED FEBRUARY , 1983 FOR THE TARGET ADDER ASSEMBLY SMD586702. TEST SPECIFICATION SMA587234 WAS USED AS A GUIDE FOR TESTING. NO DISCREPANCIES WERE FOUND IN PERFORMING THE REQUIRED TESTS. THE FOLLOWING ARE SPECIFIC REPLIES OR ANSWERS TO THE QUESTIONS ASKED IN THE TEST SPECIFICATION. OUTLINED IN THE FOLLOWING PARAGRAPHS ARE THE SMA587234 PARAGRAPH NUMBERS WHERE AN ANSWER IS NECESSARY.

SMA587234 PARAGRAPH NUMBERS

3.2.2.1.2 THE CHART SHOWN DISPLAYS THE INPUTS REQUIRED FOR COUNTING, AND THE REQUIRED OUTPUT COUNT FOR TEST NO. 1.

INPUTS

OUTPUTS

WEIGHTED NO.	8	4	2	1	
INPUTS	T2 ³	T2 ²	_{'F2} 1	T20	COUNT
	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	12
	1	1	0	1	13
	1	1	1	0	14
	1	1	1	1	15

WEIGHTED NO.	8	4	2	1	
OUTPUTS	T2 ³	T2 ²	T21 24	T2 ⁰	COUNT
	1	1	1	1	0
	1	1	1	1	0
	1	1	1	0	1
	1	1	0	1	2
	1	1	0	0	3
	1	0	1	1	4
	1	0	1	0	5
	1	0	0	1	6
	1	0	0	0	7
	0	1	1	1	8
	0	1	1	0	9
	0	1	0	1	10
	0	1	0	0	11
	0	0	1	1	12
	0	0	1	0	13
	0	0	0	1	14

THE FORM SPEC 1

2M 9-65-AINS

3.2.2.2.2 THE CHART SHOWN DISPLAYS THE INPUTS REQUIRED FOR COUNT-ING AND THE REQUIRED OUTPUT COUNT FOR TEST NO. 2.

INPUTS

WEIGHTED NO.	8	4	2	1	, a
INPUTS	T2 ³	T2 ²	T21 36	T20	COUNT
	0	0	0	0	0
	0	0	0	1	2
	0	0	1	0	
*	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	12
	1	1	0	1	13
	1	1	1	0	14
	1	1	1	1	15

OUTPUTS

WEIGHTED NO.	8	4	2	1	
OUTPUTS	T2 ³	T2 ²	T2I 24	T2 ⁰	COUNT
	1	1	0	1	2
	1	1	0	0	3
	1	0	1	0	4
	1	0	1		5
	1	0	0	1	6
	1	0	0	0	7
	0	1	1	1	8
	0	1	1	0	9
	0	1	0	1	10
	0	1	0	0	11
	0	0	1	1	12
	0	0	1	0	13
	0	0	0	1	14
	0	0	1	0	13
	0	0	0	1	14
	0	0	0	0	15

3.2.3.1.2 TEST NO. 3

BIT T REAL TIME MEASURED AT PIN 14 IS LOW AT TIME 1 BIT T REAL TIME MEASURED AT PIN 14 IS HIGH AT TIME 2

BIT T REAL TIME MEASURED AT PIN 16 IS LOW AT TIME 1
BIT T REAL TIME MEASURED AT PIN 16 IS HIGH AT TIME 2

3.2.3.2 TEST NO. 4

FRIEND REPLY MEASURED AT PIN 18 IS HIGH AT TIME 1 FRIEND REPLY MEASURED AT PIN 18 IS LOW AT TIME 2

3.2.3.3.2 TEST NO. 5

FRIEND REPLY MEASURED AT PIN 18 IS HIGH AT TIME 1 FRIEND REPLY MEASURED AT PIN 18 IS LOW AT TIME 2

3.2.3.4.2 TEST NO. 6

FRIEND REPLY MEASURED AT PIN 18 IS LOW AT TIME 1

END OF TEST RESULTS

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