TMC SPECIFICATION			NO. S1411
REV:			
COMPILED: R. Uzzo	CHECKED:	APPD:	SHEET OF
TITLE: CONTRACTOR TESTING			
SERIAL NO.			

PRODUCTION TESTING

(REFERENCE TEST SPECIFICATION)

SMA 587234

TMC SPECIFICATION			NO. S1411
REV:			
COMPILED: R. Uzzo	CHECKED:	APPD:	SHEET OF
TITLE: CONTRACTOR TESTING			

1. GENERAL INFORMATION

a) CONTRACTOR - - - - - - - - TECHNICAL MATERIEL CORP.
700 FENIMORE ROAD
MAMARONECK, NEW YORK 10543

b) CONTRACT ORDER NUMBER - DAAB07-81C-1131

c) NOMENCLATURE - - - - - - - TARGET ADDER ASSEMBLY
P/O AN/TPX - 46 (V)
DRAWING NO. SM-D-586702
NSN # 5895-00-199-7269

(EQUIPMENTS OF ESTABLISHED DESIGN)

d) SM-D-586702 FABRICATED AT:
TECHNICAL MATERIEL CORP.
700 FENIMORE ROAD
MAMARONECK, NEW YORK 10543

e) SMD-586702 - - - - - - - - STOCK NO. REPRESENTED BY
SERIAL _____

f) TESTING LOCATION: TECHNICAL MATERIEL CORP.
700 FENIMORE ROAD
MAMARONECK, NEW YORK 10543

g) TESTING DATE: - - - - - _____

h) TEST SPECIFICATIONS - - SM-A-587234

i) AMENDMENT MODIFICATION
P00002 (CHANGE NOTICE NO. 58468)

2. CROSS REFERENCING TABLE FOR SPECIFICATION SMA587234

SPECIFICATION SMA587234 REFERENCE PARAGRAPH NO.	SPECIFICATION SESCRIPTION	PAGE	PARAGRAPH NO.
3.2.1.1	POWER REQUIREMENTS	4	3.4.3
3.2.1.2	SIGNAL REQUIREMENTS	4	3.4.2
3.2.1.2.3	LOAD REQUIREMENTS	4	3.4.4
3.2.2.1	TEST NO. 1 (COUNT)	7	5.
3.2.2.2	TEST NO. 2 (COUNT)	9	7.
3.2.3.1	TEST NO. 3	11	9.1 9.2
3.2.3.2.2	TEST NO. 4	11	11.1
3.2.3.3.2	TEST NO. 5	12	13.1
3.2.3.4.2	TEST NO. 6	12	15.1

3. PURPOSE

TO ASSURE THAT THE ESTABLISHED, ACCEPTANCE TESTING FOR THE TARGET ADDER ASSEMBLY IS IN ACCORDANCE WITH TEST REQUIREMENTS, SMA587234.

3.1 TEST EQUIPMENT USED OR EQUIVALENT

a) CON AVIONICS REGULATED LV POWER SUPPLY, MODEL W32-5 TMC ID NO. 1921.

b) E-H RESEARCH LABORATORIES, PULSE GENERATOR MODEL MO139B. (CALIBRATION EXPIRES 7-6-83, CAL BY RAG CAL SERVICE)

c) TEKTRONIX OSCILLOSCOPE TYPE 541A. (CALIBRATION EXPIRES 5-19-83, CAL BY R & P ELECT.)

d) HEWLETT PACKARD ELECTRONIC COUNTER MODEL 524L. (CALIBRATION EXPIRES 5-19-83, CAL BY R & P ELECT.)

e) FLUKE MULTIMETER, MODEL 80208 SERIAL NO. 2801343. (CALIBRATION EXPIRES 7-5-83, CAL BY R & P ELECT.)

3.2 SPECIAL TEST CIRCUIT (ALL UNITS USED TO GENERATE INPUT SIGNALS TO THE TEST CIRCUIT ARE IN CALIBRATION, THE REQUIRED OUTPUT SIGNALS GENERATED BY THE TEST CIRCUIT ARE THE RESULT OF CALIBRATED INPUT SIGNALS.) TMC CONSTRUCTED THE TEST CIRCUIT, IN ORDER TO GENERATE THE REQUIRED INPUT SIGNALS TO THE SMD586702 ASSEMBLY.

(SEE FIGURE 1-1)

3.3 REFERENCE DATA USED

a) SMA587234 (TEST SPECIFICATIONS)

b) CHANGE NOTICE NO. 58468 (3 SHEETS)

c) SMD586702 (ASSEMBLY DRAWINGS)

d) SME586802 (SCHEMATIC DIAGRAM)

e) TMC TEST CIRCUIT (SCHEMATIC DIAGRAM - FIGURE 1-1 PAGE 14

3.4 TMC-PREPARED TEST CIRCUIT (SCHEMATIC FIGURE 1-1)

TMC HAS PREPARED A TEST CIRCUIT TO GENERATE THE REQUIRED INPUT SIGNALS NECESSARY IN TESTING THE TARGET ADDER ASSEMBLY. THIS TEST CIRCUIT IS HOUSED IN A .063 ALUM ALY CHASSIS 12 INCHES LONG BY 7 INCHES WIDE AND 2 INCHES DEEP. A PRINTED WIRING BOARD WAS CONSTRUCTED TO HOUSE THE CIRCUITS COMPONENTS, FIGURE 1-1 GIVES A SCHEMATIC REPRESENTATION OF THE TEST CIRCUIT. ALL COMPONENT VALUES USED IN THE TEST CIRCUIT ARE CALLED OUT IN THE SCHEMATIC DIAGRAM (FIGURE 1-1), AND ARE FOUND ADJACENT TO ALL COMPONENT SYMBOLS.

3.4.1 THE FOLLOWING ARE INPUTS DEVELOPED BY TMC'S TEST CIRCUIT.

INPUTS DEVELOPED

INPUT PIN

PULSE: NEGATIVE POLARITY: 75 n SEC ± 25n SEC (TERMINAL C)
PULSE WIDTH

PULSE: 4.1 u SEC PERIOD (TERMINAL A)

PULSE: POSITIVE POLARITY: 5.2u SEC (TERMINAL B)
PULSE WIDTH

3.4.2 SIGNAL REQUIREMENTS

PIN VARIES — HIGH LEVEL (LOGIC "1")
VOLTAGE DEVELOPED BETWEEN +2.4VDC AND +5.05VDC.

PIN VARIES — LOW LEVEL (LOGIC "0")
VOLTAGE DEVELOPED BETWEEN 0 - 0VDC AND 0 + 0.8VDC.

3.4.3 POWER REQUIREMENTS

PIN 1 AND 40 — VOLTAGE APPLIED +5±.05VDC
PIN 2 AND 41 — VOLTAGE GROUND RETURN

3.4.4 OUTPUT LOADING

THE FOLLOWING RESISTORS ARE CONNECTED AT THE OUTPUT PINS (SPECIFIED) AND +5 ± .05VDC TO ACCOMPLISH LOADING.

OUTPUT PIN	RESISTOR VALUE	LOGIC "0" LOAD	LOGIC "1" LOAD
3	270 OHM	1.6 mA	40 uA
12	270 OHM	1.6 mA	40 uA
14	270 OHM	1.6 mA	40 uA
16	270 OHM	1.6 mA	40 uA
18	270 OHM	1.6 mA	40 uA
24	270 OHM	1.6 mA	40 uA
32	270 OHM	1.6 mA	40 uA

3.4.5 INSERT PROGRAM CONNECTOR SMD587113 INTO SMD586702 ASSEMBLY.

4. TEST NO. 1 INPUTS

4.1 TARGET COUNT INPUTS

TARGET COUNT INPUTS ARE 0 to 15 for $T2^N$ or ($T2^0$, $T2^1$, $T2^2$, $T2^3$) SENSE INPUTS. $T2^0$ REPRESENTS INPUT PIN 38, $T2^1$ REPRESENTS INPUT PIN 36, $T2^2$ REPRESENTS INPUT PIN 30, $T2^3$ REPRESENTS INPUT PIN 28. A LOGIC TABLE IS PRESENTED SHOWING THE RELATION OF WEIGHTED NUMBERS TO INPUT PINS. TARGET INPUT COUNTS ARE DEVELOPED, USING THE TMC CONSTRUCTED TEST CIRCUIT (FIGURE 1-1) FOUR (4) TOGGLE SWITCHES ARE USED TO INSERT LOGIC "1" AND LOGIC "0" AS REQUIRED INTO THE INPUT PINS 28, 30, 36, 38 THUS DEVELOPING THE TARGET COUNT INPUTS 0 THROUGH 15.

LOGIC TABLE FOR INPUTS 28, 30, 36, 38

WEIGHTED NO'S	8	4	2	1	COUNT
INPUT PINS	$T2^3$	$T2^2$	$T2^1$	$T2^0$	
	28	30	36	38	
	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	12
	1	1	0	1	13
	1	1	1	0	14
	1	1	1	1	15

4.1.2 LOGIC "1" AND LOGIC "0" INPUTS

ALL LOGIC "1" AND LOGIC "0" SIGNALS ARE DEVELOPED BY THE TMC TEST CIRCUIT. REFER TO PARAGRAPH 3.4.2 (SIGNAL REQUIREMENTS) OF THIS TEST.

4.1.3 CONNECT A LOGIC "1" JUMPER TO PIN 7 ($\overline{\text{REPLY}}$)

4.1.4 CONNECT A LOGIC "1" JUMPER TO PIN 6 ($\overline{\text{BIT T + BIT B}}$)

4.1.5 CONNECT A LOGIC "0" JUMPER TO PIN 4 ($\overline{\text{BIT T + BIT B}}$)

4.1.6 CONNECT A JUMPER FROM TERMINAL "A" TO PIN 20, PIN 20 ARE THE INHIBIT PULSES WITH A 4.12 uS PERIOD.

5. TEST NO. 1 OUTPUTS

THE NUMBER ON THE $\overline{T2^N}$ OUTPUT PINS (PINS 32, 26, 12, 3) IS ONE LESS THAN THE NUMBER ON THE $T2^N$ SENSE INPUT PINS (PINS 28, 30, 36, 38). AN EXCEPTION IS WHEN THE NUMBER ON THE INPUT PINS IS ZERO. WHEN THIS OCCURS THE NUMBER ON THE OUTPUT PINS IS ALSO ZERO.

AN OVERALL LOGIC TABLE FOR TEST NO. 1 IS PRESENTED SHOWING INPUTS AND OUTPUTS. THE OUTPUT PINS 3, 12, 24 AND 32 ARE REPRESENTED ON THE TEST CIRCUIT BY (4 LAMPS). WHEN AN INPUT IS ACTIVATED, USING ANY ONE OF (4) TOGGLE SWITCHES (SEE LOGIC TABLE INPUT COLUMNS) CERTAIN OUTPUT LAMPS WILL LIGHT SIGNIFYING A LOGIC "1" CONDITION, THE LAMPS THAT DO NOT LIGHT WILL REPRESENT A "0" LOGIC CONDITION AND DUE TO THE COMPLIMENT REQUIREMENT, WILL BE USED AS THE COUNT SIGNALS. (SEE LOGIC TABLE OUTPUT COLUMNS)

LOGIC TABLE FOR TEST NO. 1

INPUTS

WEIGHTED NO.	8	4	2	1	
INPUTS	$T2^3$ 28	$T2^2$ 30	$T2^1$ 36	$T2^0$ 38	COUNT
	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	12
	1	1	0	1	13
	1	1	1	0	14
	1	1	1	1	15

OUTPUTS

WEIGHTED NO.	8	4	2	1	
OUTPUTS	$T2^3$ 3	$T2^2$ 12	$T2^1$ 24	$T2^0$ 32	COUNT
	1	1	1	1	0
	1	1	1	1	0
	1	1	1	0	1
	1	1	0	1	2
	1	1	0	0	3
	1	0	1	1	4
	1	0	1	0	5
	1	0	0	1	6
	1	0	0	0	7
	0	1	1	1	8
	0	1	1	0	9
	0	1	0	1	10
	0	1	0	0	11
	0	0	1	1	12
	0	0	1	0	13
	0	0	0	1	14

6. TEST NO. 2 INPUTS

6.1 TARGET COUNT INPUTS

TARGET COUNT INPUTS ARE 0 to 15 for $T2^N$ or ($T2^0$, $T2^1$, $T2^2$, $T2^3$) SENSE INPUTS. $T2^0$ REPRESENTS INPUT PIN 38, $T2^1$ REPRESENTS INPUT PIN 36, $T2^2$ REPRESENTS INPUT PIN 30, $T2^3$ REPRESENTS INPUT PIN 28. A LOGIC TABLE IS PRESENTED SHOWING THE RELATION OF WEIGHTED NUMBERS TO INPUT PINS. TARGET INPUT COUNTS ARE DEVELOPED, USING THE TMC CONSTRUCTED TEST CIRCUIT (FIGURE 1-1) FOUR (4) TOGGLE SWITCHES ARE USED TO INSERT LOGIC "1" AND LOGIC "0" AS REQUIRED INTO THE INPUT PINS 28, 30, 36, 38 THUS DEVELOPING THE TARGET COUNT INPUTS 0 THROUGH 15.

LOGIC TABLE FOR INPUTS 28, 30, 36, 38

WEIGHTED NO'S	8	4	2	1	COUNT
INPUT PINS	$T2^3$	$T2^2$	$T2^1$	$T2^0$	
	28	30	36	38	
	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	12
	1	1	0	1	13
	1	1	1	0	14
	1	1	1	1	15

6.1.2 LOGIC "1" AND LOGIC "0" INPUTS

ALL LOGIC "1" AND LOGIC "0" SIGNALS ARE DEVELOPED BY THE TMC TEST CIRCUIT. REFER TO PARAGRAPH 3.4.2 (SIGNAL REQUIREMENTS) OF THIS TEXT.

6.1.3 REMOVE THE LOGIC "1" JUMPER FROM PIN 7.

6.1.4 CONNECT A LOGIC "0" JUMPER TO PIN 7.

7. TEST NO. 2 OUTPUTS

THE NUMBER ON $\overline{T2^N}$ OUTPUT PINS (PINS 32, 24, 12, 3) IS TWO MORE THAN THE NUMBER ON THE $T2^N$ SENSE INPUT PINS (PINS 28, 30, 36, 38). AN EXCEPTION IS WHEN THE NUMBER ON THE INPUT PINS IS GREATER THAN OR EQUAL TO A COUNT OF 13. WHEN THIS OCCURS THE NUMBER ON THE OUTPUT PINS WILL BE THE SAME AS THE NUMBER ON THE INPUT PINS. ALL OUTPUTS ARE VIEWED AT TIME NO. 1.

AN OVERALL LOGIC TABLE FOR TEST NO. 2 IS PRESENTED SHOWING INPUTS AND OUTPUTS. THE OUTPUT PINS 3, 12, 24 and 32 ARE REPRESENTED ON THE TEST CIRCUIT BY (4 LAMPS).

WHEN AN INPUT IS ACTIVATED, USING ANY ONE OF (4) TOGGLE SWITCHES (SEE LOGIC TABLE INPUT COLUMNS) CERTAIN OUTPUT LAMPS WILL LIGHT SIGNIFYING A LOGIC "1" CONDITION THE LAMPS THAT DO NOT LIGHT WILL REPRESENT A "0" LOGIC CONDITION AND DUE TO THE COMPLIMENT REQUIREMENT, WILL BE USED AS THE COUNT SIGNALS. (SEE LOGIC TABLE (FOR TEST NO. 2) ON OUTPUT COLUMNS)

LOGIC TABLE FOR TEST # 2

INPUTS

WEIGHTED NO.	8	4	2	1	
INPUTS	$T2^3$ 28	$T2^2$ 30	$T2^1$ 36	$T2^0$ 38	COUNT
	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	12
	1	1	0	1	13
	1	1	1	0	14
	1	1	1	1	15

OUTPUTS

WEIGHTED NO.	8	4	2	1	
OUTPUTS	$\overline{T2^3}$ 3	$\overline{T2^2}$ 12	$\overline{T2^1}$ 24	$\overline{T2^0}$ 32	COUNT
	1	1	0	1	2
	1	1	0	0	3
	1	0	1	1	4
	1	0	1	0	5
	1	0	0	1	6
	1	0	0	0	7
	0	1	1	1	8
	0	1	1	0	9
	0	1	0	1	10
	0	1	0	0	11
	0	0	1	1	12
	0	0	1	0	13
	0	0	0	1	14
	0	0	1	0	13
	0	0	0	1	14
	0	0	0	0	15

END OF COUNT TEST 1 AND 2

REMOVE ALL JUMPERS

8. TEST NO. 3 INPUTS

CONNECT A JUMPER FROM TERMINAL "A" TO PIN 20. PIN 20 ARE THE INHIBIT PULSE WITH A 4.12uS PERIOD.

CONNECT A JUMPER FROM TERMINAL "C" TO PIN 22, PIN 22 IS A BIT T SENSE NEGATIVE PULSE, 75 n SEC ± 25 n SEC PULSE WIDTH.

CONNECT THE OSCILOSCOPE EXTERNAL TRIGG (+) TO PIN B. PIN B IS A SYNC PULSE USED FOR SIMPLIFYING VIEWS OF THE TIME ZONES.

CONNECT A LOGIC "O" JUMPER TO PIN 7.

9. TEST NO. 3 OUTPUTS

9.1 BIT T REAL TIME MEASURED AT PIN 14 IS LOW AT TIME 1
HIGH AT TIME 2

9.2 BIT T REAL TIME MEASURED AT PIN 16 IS HIGH AT TIME 1
LOW AT TIME 2

VIEWED ON THE OSCILLOSCOPE
CHAN A = PIN 20 CHAN B = PIN 14
CHAN B = PIN 16

10. TEST NO. 4 INPUTS

10.1 REMOVE THE JUMPER FROM PIN 22 TO TERMINAL C

10.2 REMOVE THE LOGIC "0" JUMPER TO PIN 7

10.3 CONNECT A JUMPER FROM TERMINAL "C" TO PIN 7

10.4 CONNECT A LOGIC "1" JUMPER TO PIN 10

10.5 CONNECT A LOGIC "0" JUMPER TO PIN 8

11. TEST NO. 4 OUTPUTS

11.1 FRIEND REPLY MEASURED AT PIN 18 IS HIGH AT TIME 1
LOW AT TIME 2

VIEWED ON THE OSCILLOSCOPE
CHAN A + PIN 20 CHAN B = 18

12. TEST NO. 5 INPUTS

12.1 REMOVE A LOGIC "1" JUMPER TO PIN 10

12.2 CONNECT A LOGIC "0" JUMPER TO PIN 10

12.3 REMOVE A LOGIC "0" JUMPER TO PIN 8

12.4 CONNECT A LOGIC "1" JUMPER TO PIN 8

13. TEST NO. 5 OUTPUTS

13.1 FRIEND REPLY MEASURED AT PIN 18 IS HIGH AT TIME 1
LOW AT TIME 2

14. TEST NO. 6 INPUTS

14.1 REMOVE THE JUMPER FROM LOGIC "0" TO PIN 10

14.2 REMOVE THE JUMPER FROM LOGIC "1" TO PIN 8

14.3 CONNECT PINS 10 AND 8 TO PIN D, PIN D IS A POSITIVE PULSE OF 5.6uS LOW DURING TIME 3

15. TEST NO. 6 OUTPUTS

15.1 FRIEND REPLY MEASURED AT PIN 18 IS LOW AT TIME 1

ALL TEST REQUIREMENTS FOR THE POST TARGET ADDER ASSEMBLY SMD586702 HAVE BEEN COMPLIED WITH, IN ACCORDANCE WITH "TEST REQUIREMENTS SMA587234."

ALL TEST PROCEDURES SPECIFIED IN THIS TEXT WILL BE IMPLEMENTED DURING TESTING OF ALL SMD586702 ASSEMBLIES.

DATE TEST WAS PERFORMED_____

TESTERS SIGNATURE_____ SERIAL NO._____

WITNESSED BY

GOVERNMENT REPRESENTIVE_____

DATE_____