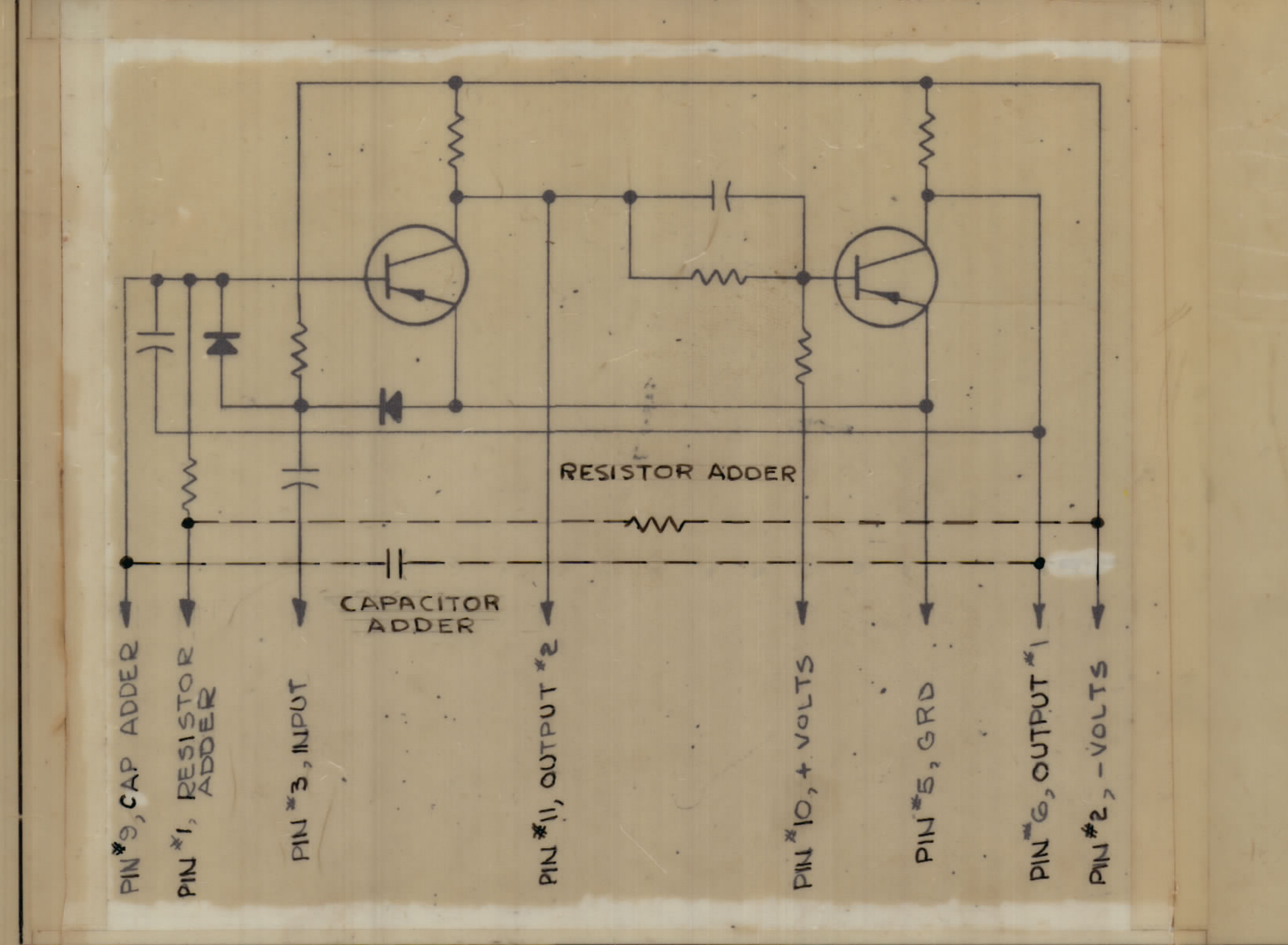
REVISIONS

SYM	DESCRIPTION	DATE	E.M.N.	DRAFT	CHKD	APPD
X1	"OS" AND "T.G" TYPICAL COMPONENTS ADDED TIMING CIRCUIT COMPONENT VALUES ADDED	10/14/65				
X2	ON OS CIRCUIT CAPACITOR ADDER WAS CONNECTED FROM PIN 9 & PIN 2 – ON OS-2 Z3 C2 WAS 1 µF – ON CHART MODULE DESC. FOR CF 5 NAG-8 & AG-8 CLARIFIED SEE SHEETS 2 3 & 4	10-26-65	X2	GDL		
Ø	ORIGINAL RELEASE	11-2-65	Ø	GDL		
A	SEE SHEET 2 OF 4 AND 4 OF 4	12/10/65	15272			

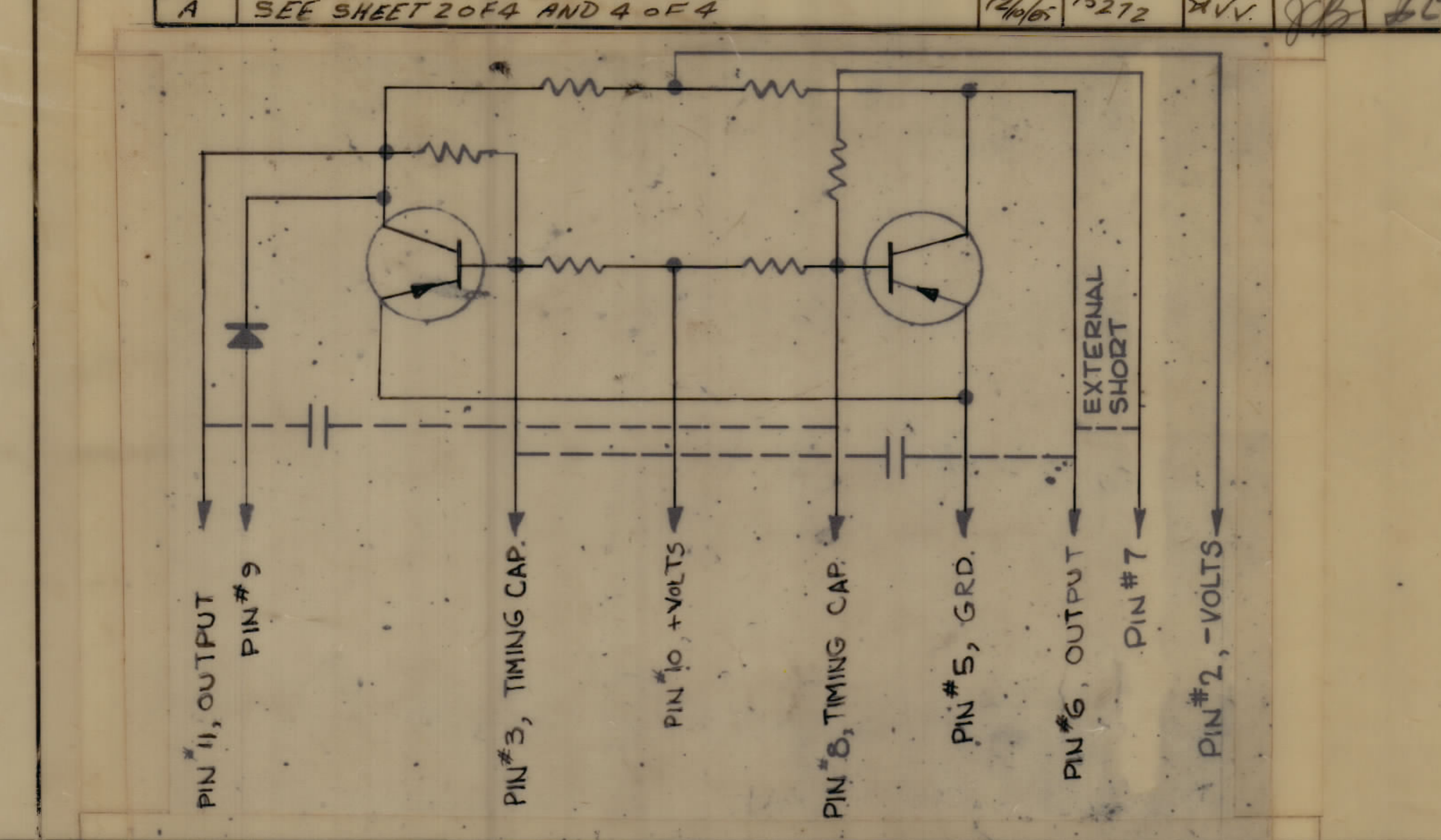
CARDS USED

PART NO.	DESCRIPTION	CON. NO.	LOCATION	B+ INPUT	B- INPUT	GROUND
PC127/A3694	INITIAL RESET CIRCUIT	J5007	SHEET 2	PIN 5	PIN 37	1,2,43,44
PC220/A4295	SERIAL TO PARALLEL CLOCK CIRCUIT	J5008	2	5	37	1,2,43,44
PC221/A4294	SERIAL TO PARALLEL SHIFT REGISTER	J5009	2	5	37	1,2,43,44
PC218/A4254	STUNTING CARD, DOUBLE CHARACTER	J5010	3	5	37	1,2,43,44
PC169/A3812	ADVANCE, TUNE COMPLETE, BOY RELAY CKT.	J5011	1	5	37	1,2,43,44
PC175/A3823	ADVANCE PRIME TIMING CIRCUIT	J5012	2	5	37	1,2,43,44
PC171/A3820	MEMORY CORE INPUT SHIFT REGISTER	J5013	4	5	37	1,2,43,44
PC173/A3821	PRIME CIRCUIT CARD	J5014	3	5	37	1,2,43,44
PC176/A3824	ADVANCE "O" & "E" CIRCUIT	J5015	3	5	37	1,2,43,44
PC182/A3639	MEMORY CORE REGISTER	J5016	4	6	2	18
		J5017	4	6	2	18
		J5018	4	6	2	18
		J5019	4	6	2	18
PC182/A3639	MEMORY CORE REGISTER	J5020	4	6	2	18
PC158/A3800	DRIVE CIRCUIT FOR DECODER RELAYS	J5021	SHEET 4	5	37	1,2,43,44



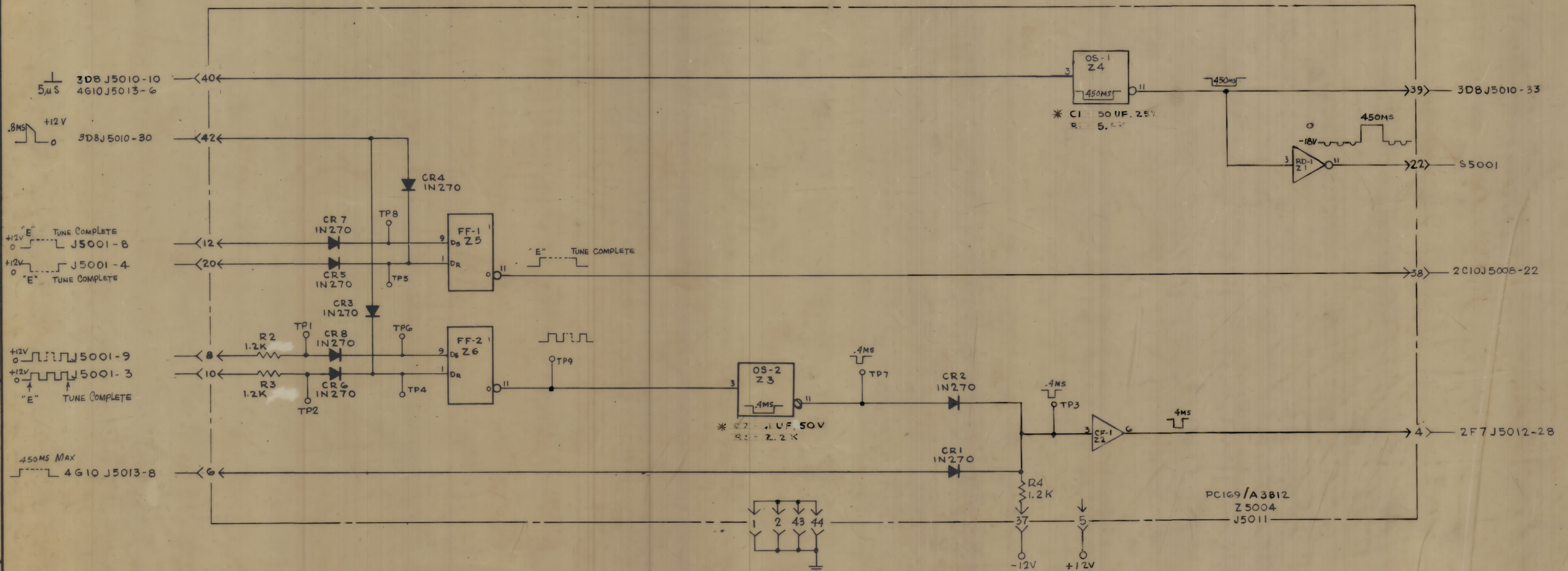
TYPICAL "OS" CIRCUIT

NOTE: * INDICATES VALUES OF RESISTOR & CAPACITOR USED WHEN CALLED FOR BENEATH RESPECTIVE "OS" MODULES IN DIAGRAM.

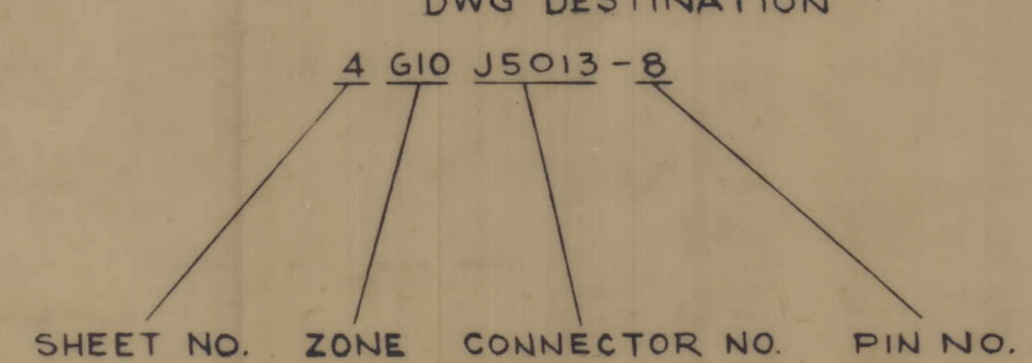


TYPICAL "TG" CIRCUIT

NOTE: ** INDICATES VALUES OF CAPACITORS USED WHEN CALLED FOR BENEATH RESPECTIVE "TG" MODULE IN DIAGRAM. QTY OF CAPACITORS MAY VARY WHEN IT BECOMES NECESSARY TO PARALLEL TO ARRIVE AT DESIRED VALUE.



DWG DESTINATION



– UNLESS OTHERWISE SPECIFIED –

1- ALL RESISTOR VALUES ARE IN OHMS, 1/2 WATT.

LAST NO. USED, MODULE DESIG. CODE	
NO USED	MODULE DESCRIPTION
FF-23	FLIP FLOP
OS-16	ONE SHOT
CF-5	COMPLEMENTARY EMITTER FOLLOWER
RD-2	RELAY DRIVER
IV-2	INVERTER
PF-10	POSITIVE EMITTER FOLLOWER
NAG-8	NAND GATE
NA-11	NON INVERTING AMPLIFIER
NG-2	NOR GATE
TG-2	TIMING GENERATOR
AG-8	AND GATE

REQ'D	ITEM	PART NUMBER	DESCRIPTION	SYMBOL
EATON		LIST OF MATERIAL		

MATERIAL

FINISH

THE TECHNICAL MATERIEL CORP.
MAMARONECK, NEW YORK

TITLE: DIAGRAM, LOGIC DETAILED RTMU-2

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

TOLERANCES — DECIMALS: X ± .05, XX ± .01, XXX ± .005 — FRACTIONS: ± 1/64 — ANGLES: ± 0° 30'

DRAWN — DATE
CHECKED — DATE 10/6/65
ELECT. DES. — DATE 10/29/65
MECH. DES. — DATE
FINAL APPROVAL F E Eaton — DATE 11/2/65

CK1044 — REV. LTR. A

SHEET 1 OF 4

M/L — 10/18/65

REVISIONS

SYM	DESCRIPTION	DATE	E.M.N. NO	DRAFT	CHKD	APPD
X1	*"OS" & **"TG" COMPONENT VALUES ADDED	10/14/65		A.V.V.		
X2	ON TG1 Z3 C4 WAS .65uf, ON OS-10 Z2 C2 WAS C3, ON OS-8 Z1 R1 WAS 33 K - SEE SHEETS 1, 3 & 4	10-26-65	X2			
Ø	ORIGINAL RELEASE	11-2-65	Ø	G.D.L.		
A	50V ADDED (SEE SHEET 4 OF 4	12/10/65	15272	A.V.V.		

- UNLESS OTHERWISE SPECIFIED -

1 - ALL RESISTOR VALUES ARE IN OHMS, 1/2 WATT.

REQ'D	ITEM	PART NUMBER	DESCRIPTION	SYMBOL
EATON		LIST OF MATERIAL		

MATERIAL

FINISH

THE TECHNICAL MATERIEL CORP.
MAMARONECK, NEW YORK

TITLE: DIAGRAM, LOGIC, DETAILED
RTMU-2

✓ UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

DECIMALS: .X ± .05, .XX ± .01, .XXX ± .005 — TOLERANCES — FRACTIONS ± 1/64, ANGLES ± 0° 30'

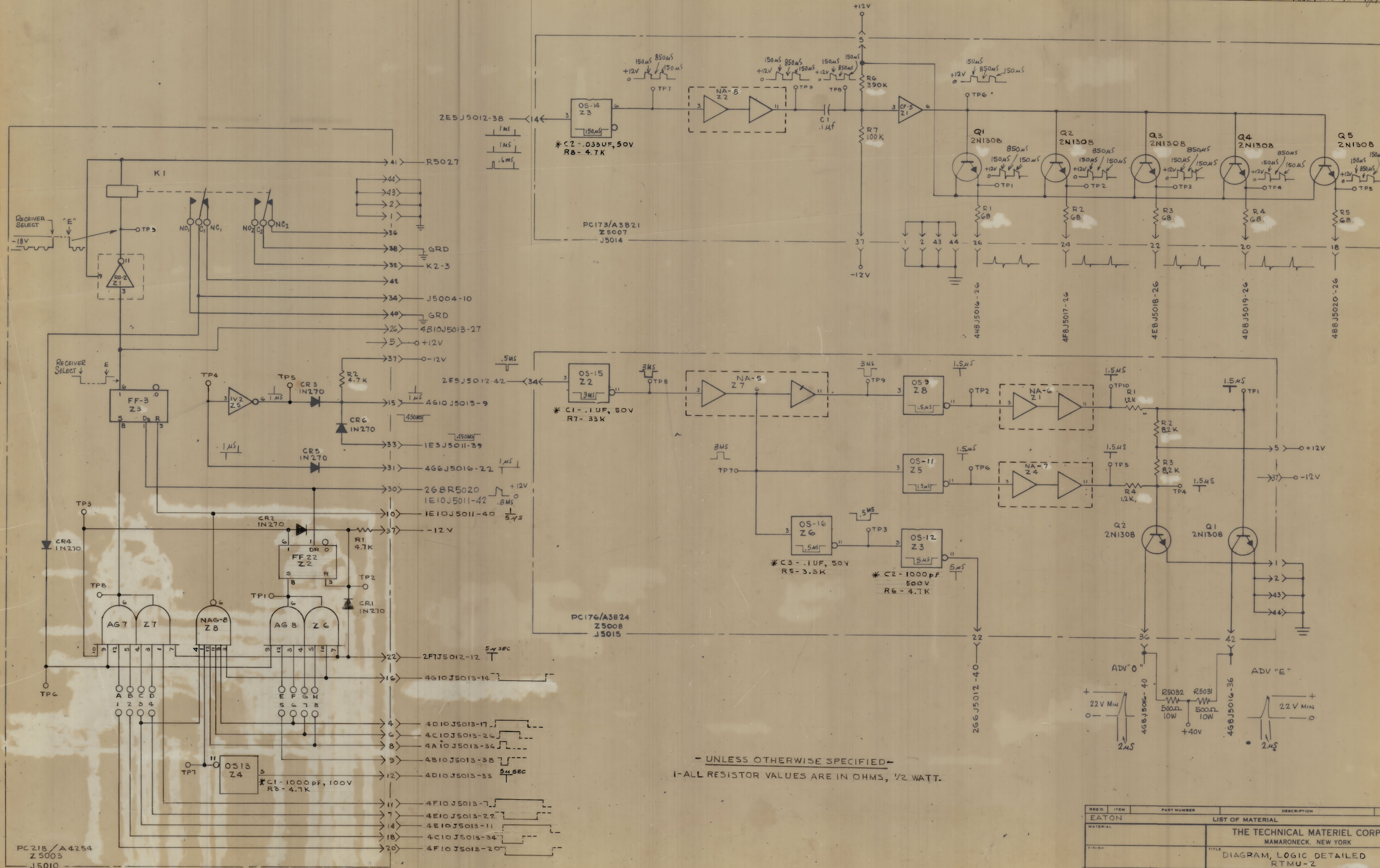
DRAWN | DATE
CHECKED | DATE 10/6/65
ELECT. DES. | DATE 10/29/65
MECH. DES. | DATE
M/L | 10-18-65

FINAL APPROVAL: F E Eaton | DATE 11/2/65

CK1044 | 4

SHEET 2 OF 4 | REV LTR.

SYM	DESCRIPTION	DATE	E.M.N. NO.	DRAFT	CHKD	APPD
REVISIONS						
X1	* "OS" COMPONENT VALUES ADDED	10/14/65				
X2	ON OS-16 Z6 R5 WAS 33K - SEE SHEETS 1, 2 & 4	10-26-65		G.D.L		
Ø	ORIGINAL RELEASE	11-2-65	Ø	G.D.L		
A	SEE SHEET 2 OF 4 AND 4 OF 4	12/10/65	15272			



- UNLESS OTHERWISE SPECIFIED -

1 - ALL RESISTOR VALUES ARE IN OHMS, 1/2 WATT.

REQ'D	ITEM	PART NUMBER	DESCRIPTION	SYMBOL
EATON			LIST OF MATERIAL	

THE TECHNICAL MATERIEL CORP.
MAMARONECK, NEW YORK

TITLE: DIAGRAM, LOGIC DETAILED
RTMU-2

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

TOLERANCES: DECIMALS .X ± .05, .XX ± .01, .XXX ± .005; FRACTIONS ± 1/64; ANGLES ± 0° 30'

DRAWN	DATE	FINAL APPROVAL	DATE
CHECKED	DATE 10/6/65		11/2/65
ELECT. DES.	DATE 10/29/65	CK1044	A
MECH. DES.	DATE	SHEET 3 OF 4	REV. LTR.
M/L J.J. MUNFORD	10-18-65		

REVISIONS

SYM	DESCRIPTION	DATE	E.M.N. NO.	DRAFT	CHKD	APPD
X1	*"OS" & **"TG" COMPONENT VALUES ADDED	10/19/65		D.V.V.		
X2	J5001-2 WAS J5001 - SEE SHEETS 1, 2 & 3	10-26-65		G.D.L		
Ø	ORIGINAL RELEASE	11-2-65	Ø	G.D.L		
A	C4 DELETED (SEE SHEET 2 OF 4)	12 10 65	15272	D.V.V.		

- UNLESS OTHERWISE SPECIFIED -
1. ALL RESISTOR VALUES ARE IN OHMS, 1/2 WATT.

REQ'D	ITEM	PART NUMBER	DESCRIPTION	SYMBOL
EATON		LIST OF MATERIAL		

MATERIAL

FINISH

THE TECHNICAL MATERIEL CORP.
MAMARONECK, NEW YORK

TITLE: DIAGRAM, LOGIC DETAILED RTMU-2

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

TOLERANCES: DECIMALS X ± .05, XX ± .01, XXX ± .005; FRACTIONS ± 1/64; ANGLES ± 0° 30'

DRAWN / DATE
CHECKED / DATE 10/6/65
ELECT DES / DATE 10/29/65
MECH DES / DATE
FINAL APPROVAL / DATE 11/2/65

CK1044 — REV LTR A

SHEET 4 OF 4

M/L J. MUNFORD 10-18-65